

TMS320F2837xS Delfino™ Microcontrollers

1 Device Overview

1.1 Features

- TMS320C28x 32-Bit CPU
 - 200 MHz (5-ns Cycle Time)
 - IEEE 754 Single-Precision Floating-Point Unit (FPU)
 - Trigonometric Math Unit (TMU)
 - Viterbi/Complex Math Unit (VCU-II)
 - 16 × 16 and 32 × 32 Multiply and Accumulate (MAC) Operations
 - 16 × 16 Dual MAC
 - Three 32-Bit CPU Timers
 - Harvard Bus Architecture
 - Fast Interrupt Response and Processing
 - Unified Memory Programming Model
- Programmable Control Law Accelerator (CLA)
 - 200 MHz (5-ns Cycle Time)
 - 32-Bit Floating-Point Math Accelerator (IEEE 754 Single Precision)
 - Executes Code Independently of Main CPU
- On-Chip Memory
 - Up to 1MB of Flash, Up to 164KB of RAM
 - Boot ROM (64KB)
 - Serial Peripheral Interface (SPI), Inter-Integrated Circuit (I²C), Controller Area Network (CAN), and Parallel I/O Software Boot Modes
 - Standard Math Tables
- System Peripherals
 - Two External Memory Interfaces (EMIFs) With ASRAM and SDRAM Support
 - 6-Channel Direct Memory Access (DMA) Controller
 - Up to 169 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins With Input Filtering
- Communications Peripherals
 - USB 2.0 + PHY Port
 - Support for 12-Pin 3.3 V-Compatible Universal Parallel Port (uPP) Interface
 - Two CAN-Bus Ports (32 Mailboxes Each)
 - Three High-Speed (40-MHz) SPI Ports With 16-Level FIFO, DMA Support, and CLA-Accessible
 - Two Multichannel Buffered Serial Ports (McBSPs)
 - Up to Four Serial Communications Interfaces (SCIs)
 - Two I²C Interfaces
- Analog Subsystem
 - Up to Four Dual-Mode Analog-to-Digital Converters (ADCs)
 - 16-Bit Mode
 - 1.1 MSPS Each (up to 4.4-MSPS System)
 - Differential
 - External Reference
 - Up to 12 External Channels
 - 12-Bit Mode
 - 3.5 MSPS Each (up to 14-MSPS System)
 - Single-Ended or Differential
 - External Reference
 - Up to 24 External Channels
 - Single Sample-and-Hold (S/H) on Each ADC
 - Integrated Post-Processing of ADC Conversions
 - Saturating Offset Calibration
 - Error From Setpoint Calculation
 - High, Low, and Zero-Crossing Compare, With Interrupt Capability
 - Trigger-to-Sample Delay Capture
 - Analog Comparator/Digital-to-Analog Converter (DAC) Subsystem With Glitch Filter, for Windowed Trip Monitor and Peak Current Mode Control (PCMC) Interfaces
 - Eight Windowed Comparators With 12-Bit DAC References
 - Three 12-Bit Buffered DAC Outputs
- Enhanced Control Peripherals
 - Up to 24 PWM Channels With Enhanced Features
 - Up to 16 High-Resolution Pulse Width Modulator (HRPWM) Channels
 - High Resolution on Both A and B Channels of 8 PWM Modules
 - Dead-Band Support (on Both Standard and High Resolution)
 - Six Enhanced Capture (eCAP) Modules
 - Up to Three Enhanced Quadrature Encoder Pulse (eQEP) Modules
 - Two Sigma-Delta Filter Module (SDFMs) With up to 8 Input Channels, and Pulse Width Modulator (PWM) Synchronization



- Expanded Peripheral Interrupt (ePIE) Block
 - Supports up to 192 Peripheral Interrupts
 - GPIO Pins can be Connected to 5 Core Interrupts
- JTAG Boundary Scan Support
 - IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture
- Advanced Emulation Features
 - Analysis and Breakpoint Functions
 - Two Hardware Breakpoints
 - Real-Time Debug via Hardware
- Dual-Zone Security
 - 128-Bit Security Key and Lock
 - Protects Flash, One-Time Programmable (OTP) Memory, and RAM Blocks
- Safety and Reliability Features
 - Error Correction Code (ECC) on Flash, ECC or Parity on RAMs
 - Missing Clock Detection
 - Programmable Built-In Self-Test (for Memory)
- Low-Power Modes and Power Savings
 - IDLE, STANDBY, HALT, and HIBERNATE Modes Supported
 - Disable Individual Peripheral Clocks
- Clock and System Control
 - Two Internal Zero-Pin 10-MHz Oscillators
 - On-Chip Crystal Oscillator and External Clock Input
 - Watchdog Timer Module
 - Missing Clock Detection Circuitry
- 1.2-V Core, 3.3-V I/O Design
- Development Support Includes
 - ANSI C/C++ Compiler/Assembler/Linker
 - Code Composer Studio™ Integrated Development Environment (IDE)
 - SYS/BIOS
 - Digital Motor Control and Digital Power Libraries
 - FPU and VCU Optimized Libraries
 - TMU Native Compiler Support
- Package Options:
 - Lead-Free, Green Packaging
 - 337-Ball New Fine Pitch Ball Grid Array (nFBGA) [ZWT Suffix]
 - 176-Pin PowerPAD™ Thermally Enhanced Low-Profile Quad Flatpack (HLQFP) [PTP Suffix]
 - 100-Pin PowerPAD Thermally Enhanced Thin Quad Flatpack (HTQFP) [PZP Suffix]
- Temperature Options:
 - T: –40°C to 105°C
 - S: –40°C to 125°C
 - Q: –40°C to 125°C (Q100 Qualification for Automotive Applications)

1.2 Applications

- Industrial Drives
- Solar Micro Inverters and Converters
- Radar
- Digital Power
- Smart Metering
- Automotive Transportation
- Power Line Communications
- Software-Defined Radio

1.3 Description

The Delfino™ TMS320F2837xS is a powerful 32-bit floating-point microcontroller unit (MCU) that lets designers consolidate control architectures and eliminate multiprocessor use in high-end systems.

The real-time control subsystem is based on TI's 32-bit C28x floating-point CPU, which provides 200 MHz of signal processing performance. The C28x CPU is further boosted by the new TMU accelerator, which enables fast execution of algorithms with trigonometric operations common in transforms and torque loop calculations; and the VCU accelerator, which reduces the latency for complex math operations common in encoded applications.

The F2837xS features a real-time control accelerator, also known as CLA. The CLA provides an additional floating-point accelerator used to run parallel time-critical control algorithms, providing bandwidth for the C28x to focus on system tasks.

The TMS320F2837xS supports up to 1MB of on-board flash memory with ECC and up to 164KB of SRAM. Two 128-bit secure zones are also available on the CPU for code protection.

Performance analog and control peripherals are also integrated on the F2837xS MCU to further enable system consolidation. Four independent 16-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. New sigma-delta peripherals enable isolated current shunt measurements and windowed comparators allow protection of power stage when current limit conditions are exceeded or not met. Other analog and control peripherals include DACs, PWMs, eCAPs, eQEPs, and other peripherals.

Connectivity peripherals such as dual EMIFs, dual CAN 2.0 interfaces, and a new uPP extend the performance of the F2837xS. The uPP is a new feature to the TMS320C2000™ MCUs and supports high-speed parallel connection to FPGAs or other processors with similar uPP interfaces. Lastly, a USB 2.0 host port with MAC and PHY lets users easily add USB connectivity to their application.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE
TMS320F28377SZWT	nFBGA (337)	16.0 mm x 16.0 mm
TMS320F28376SZWT	nFBGA (337)	16.0 mm x 16.0 mm
TMS320F28375SZWT	nFBGA (337)	16.0 mm x 16.0 mm
TMS320F28374SZWT	nFBGA (337)	16.0 mm x 16.0 mm
TMS320F28377SPTP	HLQFP (176)	24.0 mm x 24.0 mm
TMS320F28376SPTP	HLQFP (176)	24.0 mm x 24.0 mm
TMS320F28375SPTP	HLQFP (176)	24.0 mm x 24.0 mm
TMS320F28374SPTP	HLQFP (176)	24.0 mm x 24.0 mm
TMS320F28377SPZP	HTQFP (100)	14.0 mm x 14.0 mm
TMS320F28376SPZP	HTQFP (100)	14.0 mm x 14.0 mm
TMS320F28375SPZP	HTQFP (100)	14.0 mm x 14.0 mm
TMS320F28374SPZP	HTQFP (100)	14.0 mm x 14.0 mm

(1) For more information on these devices, see [Section 8](#), Mechanical Packaging and Orderable Information.

1.4 Functional Block Diagram

Figure 1-1 shows the CPU system and associated peripherals.

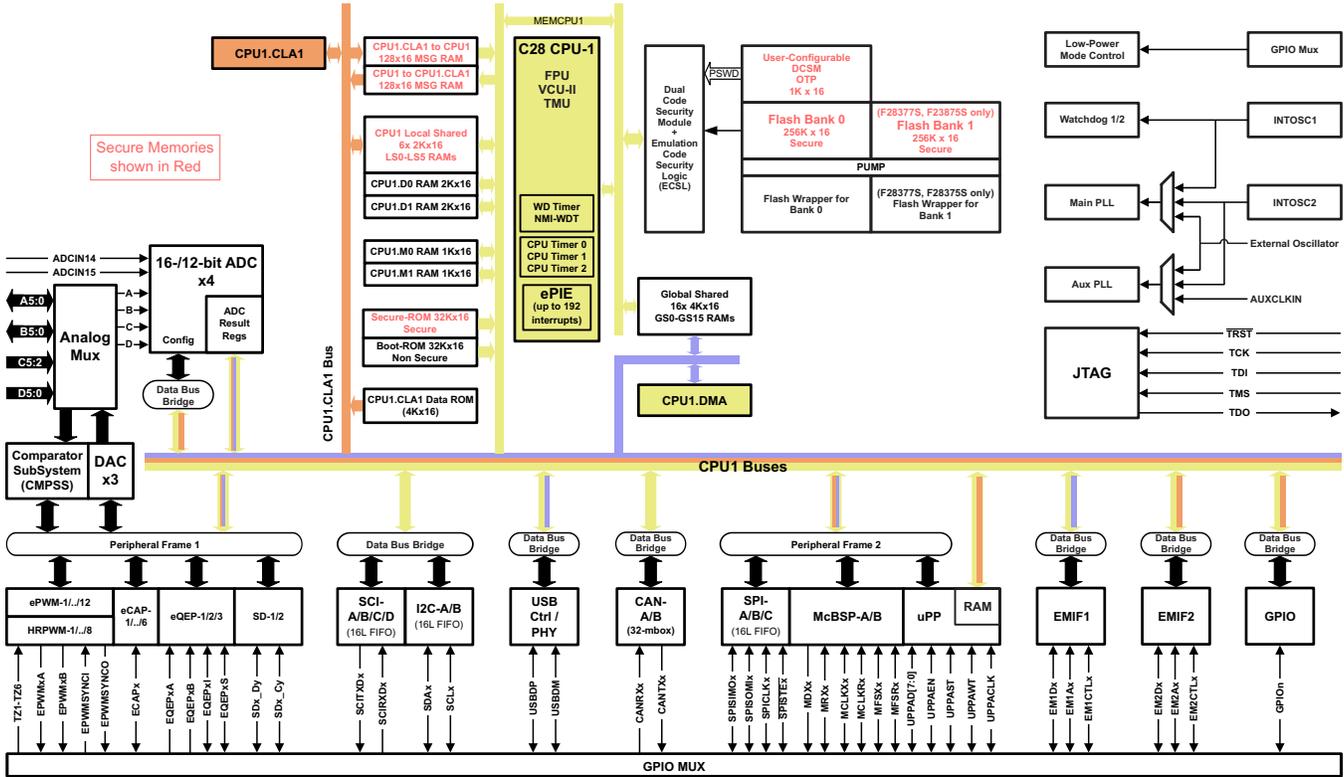


Figure 1-1. Functional Block Diagram

ADVANCE INFORMATION

Table of Contents

1	Device Overview	1			56
	1.1 Features	1		6.1 Functional Block Diagram	56
	1.2 Applications	2		6.2 Memory Maps	58
	1.3 Description	3		6.3 Device Identification Registers	63
	1.4 Functional Block Diagram	4		6.4 Bus Architecture – Peripheral Connectivity	64
2	Revision History	6		6.5 CPU and System Control	65
3	Device Comparison	7		6.6 Analog Peripherals	77
4	Terminal Configuration and Functions	9		6.7 Control Peripherals	86
	4.1 Signal Descriptions	15		6.8 Communications Peripherals	95
	4.2 Pin Multiplexing	39	7	Device and Documentation Support	107
5	Specifications	43		7.1 Device Support	107
	5.1 Absolute Maximum Ratings	43		7.2 Documentation Support	109
	5.2 Handling Ratings	43		7.3 Related Links	110
	5.3 Recommended Operating Conditions	43		7.4 Community Resources	110
	5.4 Electrical Characteristics	44		7.5 Trademarks	110
	5.5 Timing and Switching Characteristics	45		7.6 Electrostatic Discharge Caution	110
	5.6 Power Management	48		7.7 Glossary	110
	5.7 Clocking	49	8	Mechanical Packaging and Orderable Information	111
6	Detailed Description	56		8.1 Packaging Information	111

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2014	*	Initial Release

ADVANCE INFORMATION

3 Device Comparison

Table 3-1. Device Comparison Table

FEATURE ⁽¹⁾		28377S			28376S			28375S			28374S		
Package Type (ZWT is an nFBGA package. PTP is an HLQFP package. PZP is an HTQFP package.)		337- Ball ZWT	176- Pin PTP	100- Pin PZP									
Processor speed (MHz)		200											
FPU		Yes											
VCU-II		Yes											
TMU – Type 0		Yes											
CLA – Type 1		1											
6-Channel DMA – Type 0		1											
Flash (16-bit words)		512KW			256KW			512KW			256KW		
RAM (16-bit words)	Dedicated and Local Shared RAM	18KW											
	Global Shared RAM	64KW			48KW			64KW			48KW		
	Total RAM	82KW			66KW			82KW			66KW		
Code security for on-chip Flash, RAM, and OTP blocks		Yes											
Boot ROM		Yes											
OTP memory (16-bit words)		2KW											
Enhanced Pulse Width Modulator (ePWM) Type-4 channels		24	15		24	15		24	15		24	15	
High-resolution ePWM Type-4 channels		16	9		16	9		16	9		16	9	
eCAP inputs – Type 0		6											
eQEP modules – Type 0		3	2		3	2		3	2		3	2	
32-bit CPU timers		3											
Watchdog timers		1											
Nonmaskable Interrupt Watchdog (NMIWD) timers		1											
ADC 16-bit mode	MSPS	1.1						–					
	Conversion Time (ns)	915						–					
	Input pins	24	20	14	24	20	14	–					
	Channels (differential)	12	9	7	12	9	7	–					
ADC 12-bit mode	MSPS	3.5											
	Conversion Time (ns)	290											
	Input pins	24	20	14	24	20	14	24	20	14	24	20	14
	Channels (differential/single-ended)	12/24	9/20	7/14	12/24	9/20	7/14	12/24	9/20	7/14	12/24	9/20	7/14
Number of 16-bit or 12-bit ADCs		4		2	4		2	–					
Number of 12-bit only ADCs		–						4		2	4		2
Temperature sensor		1											
CMPSS (each CMPSS has two Comparators and two internal DACs)		8	4		8	4		8	4		8	4	
Buffered DAC		3											
SDFM channels		8											
I ² C – Type 0		2											
McBSP – Type 1		2											
uPP		1											
CAN – Type 0		2											
SPI – Type 2		3											
SCI – Type 0		4	3		4	3		4	3		4	3	
Universal Serial Bus (USB) – Type 0		1											

Table 3-1. Device Comparison Table (continued)

FEATURE ⁽¹⁾		28377S			28376S			28375S			28374S		
Package Type (ZWT is an nFBGA package. PTP is an HLQFP package. PZP is an HTQFP package.)		337- Ball ZWT	176- Pin PTP	100- Pin PZP									
EMIF	EMIF1 16/32-bit	1	-	-	1	-	-	1	-	-	1	-	-
	EMIF2 16-bit	1	-	-	1	-	-	1	-	-	1	-	-
On-chip crystal oscillator/External clock input		1											
0-pin internal oscillator		2											
I/O pins (shared)	GPIO	169	97	41	169	97	41	169	97	41	169	97	41
External interrupts		5											
Free-Air Temperature (T _A) options	T: -40°C to 105°C	Yes											
	S: -40°C to 125°C	Yes											
	Q: -40°C to 125°C ⁽²⁾	Yes											
Product status ⁽³⁾		TMX											

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module.

(2) "Q" refers to Q100 qualification for automotive applications.

(3) The "TMX" product status denotes an experimental device that is not necessarily representative of the final device's electrical specifications.

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4 Terminal Configuration and Functions

Figure 4-1 to Figure 4-4 show in four quadrants the terminal assignments on the 337-ball ZWT New Fine Pitch Ball Grid Array. Figure 4-5 shows the pin assignments on the 176-pin PTP PowerPAD Thermally Enhanced Low-Profile Quad Flatpack. Figure 4-6 shows the pin assignments on the 100-pin PZP PowerPAD Thermally Enhanced Thin Quad Flatpack.

	1	2	3	4	5	6	7	8	9	10	
W	V _{SSA}	ADCINB1	ADCINB3	ADCINB5	V _{REFHIB}	V _{REFLOD}	V _{SS}	V _{DDIO}	GPIO128	GPIO116	W
V	V _{REFHIA}	ADCINB0	ADCINB2	ADCINB4	V _{REFHID}	V _{REFLOB}	V _{SSA}	GPIO124	GPIO127	GPIO131	V
U	ADCINA0	ADCINA2	ADCINA4	ADCIN15	ADCIND1	ADCIND3	ADCIND5	GPIO123	GPIO126	GPIO130	U
T	ADCINA1	ADCINA3	ADCINA5	ADCIN14	ADCIND0	ADCIND2	ADCIND4	GPIO122	GPIO125	GPIO129	T
R	V _{REFHIC}	V _{REFLOA}	ADCINC2	ADCINC4	V _{SSA}	V _{DDA}	V _{SS}	V _{SS}	V _{DDIO}	V _{DD}	R
P	V _{SSA}	V _{REFLOC}	ADCINC3	ADCINC5	V _{SSA}	V _{DDA}	V _{SS}	V _{SS}	V _{DDIO}	V _{DD}	P
N	V _{SS}	GPIO109	GPIO114	GPIO113	V _{SS}	V _{SS}	7 N	8	9	10	N
M	V _{DDIO}	GPIO110	GPIO112	GPIO111	V _{DDIO}	V _{DDIO}	M	V _{SS}	V _{SS}	V _{SS}	M
L	GPIO27	GPIO106	GPIO107	GPIO108	V _{SS}	V _{SS}	L	V _{SS}	V _{SS}	V _{SS}	L
K	GPIO26	GPIO25	GPIO24	GPIO23	V _{DD}	V _{DD}	K	V _{SS}	V _{SS}	V _{SS}	K
	1	2	3	4	5	6		8	9	10	

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A. Only the GPIO function is shown on GPIO terminals. See Table 4-1 for the complete, muxed signal name.

Figure 4-1. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant A]

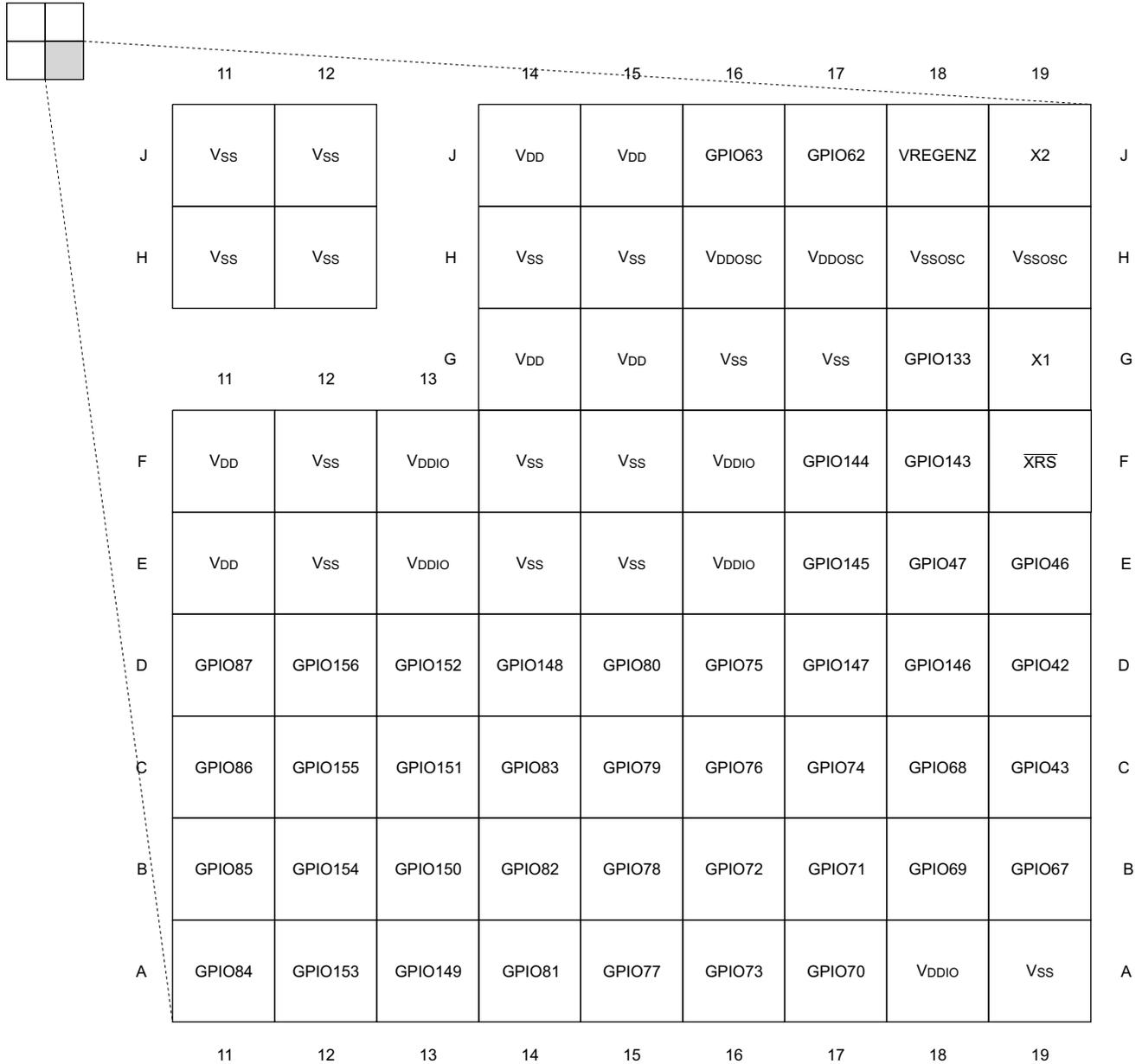
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	11	12	13	14	15	16	17	18	19		
W	GPIO29	FLT1	TDI	TMS	TDO	GPIO121	GPIO39	GPIO132	V _{SS}	W	
V	GPIO28	GPIO115	FLT2	$\overline{\text{TRST}}$	TCK	GPIO36	GPIO40	GPIO134	V _{DDIO}	V	
U	GPIO31	GPIO117	GPIO32	GPIO34	GPIO120	GPIO37	GPIO41	GPIO135	ERRORSTS	U	
T	GPIO30	GPIO118	GPIO33	GPIO35	GPIO119	GPIO38	GPIO136	GPIO137	GPIO138	T	
R	V _{DD3VFL}	V _{DD3VFL}	V _{DD}	V _{SS}	V _{SS}	GPIO48	GPIO49	GPIO50	GPIO51	R	
P	V _{SS}	V _{SS}	V _{DD}	V _{SS}	V _{SS}	GPIO52	GPIO53	GPIO54	GPIO55	P	
	11	12	13	N	V _{DDIO}	V _{DDIO}	GPIO56	GPIO58	GPIO57	GPIO139	N
M	V _{SS}	V _{SS}	M	V _{SS}	V _{SS}	GPIO59	GPIO60	GPIO141	GPIO140	M	
L	V _{SS}	V _{SS}	L	V _{DDIO}	V _{DDIO}	GPIO61	GPIO64	V _{SS}	GPIO142	L	
K	V _{SS}	V _{SS}	K	V _{SS}	V _{SS}	GPIO65	GPIO66	GPIO44	GPIO45	K	

	11	12	14	15	16	17	18	19
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A. Only the GPIO function is shown on GPIO terminals. See Table 4-1 for the complete, muxed signal name.

Figure 4-2. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant B]



ADVANCE INFORMATION

A. Only the GPIO function is shown on GPIO terminals. See [Table 4-1](#) for the complete, muxed signal name.

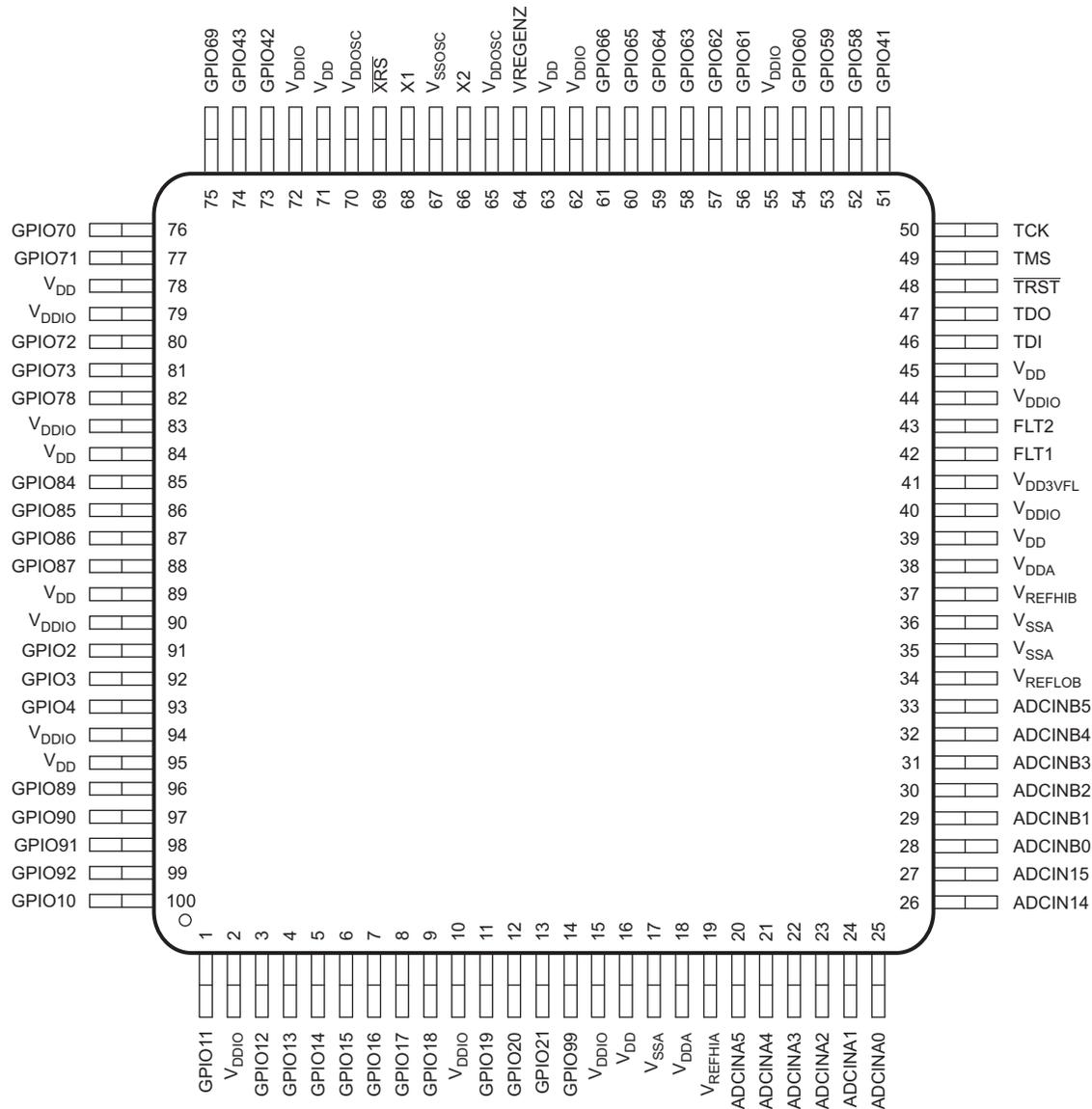
Figure 4-3. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant C]



	1	2	3	4	5	6		8	9	10	
J	GPIO103	GPIO104	GPIO105	GPIO22	Vss	Vss	J	Vss	Vss	Vss	J
H	GPIO100	GPIO101	GPIO102	NC	VDDIO	VDDIO	H	Vss	Vss	Vss	H
G	GPIO99	GPIO8	GPIO9	VDDIO	VDDIO	VDDIO	G	7	8	9	10
F	GPIO98	GPIO20	GPIO21	VDDIO	Vss	Vss	VDDIO	Vss	VDD	VDDIO	F
E	GPIO16	GPIO17	GPIO18	GPIO19	Vss	Vss	VDDIO	Vss	VDD	VDDIO	E
D	GPIO13	GPIO14	GPIO15	GPIO168	GPIO166	GPIO89	GPIO5	GPIO1	GPIO162	GPIO159	D
C	GPIO11	GPIO12	GPIO96	GPIO167	GPIO165	GPIO88	GPIO4	GPIO0	GPIO161	GPIO158	C
B	VDDIO	GPIO10	GPIO95	GPIO93	GPIO91	GPIO7	GPIO3	GPIO164	GPIO160	GPIO157	B
A	Vss	GPIO97	GPIO94	GPIO92	GPIO90	GPIO6	GPIO2	GPIO163	VDDIO	Vss	A
	1	2	3	4	5	6	7	8	9	10	

A. Only the GPIO function is shown on GPIO terminals. See [Table 4-1](#) for the complete, muxed signal name.

Figure 4-4. 337-Ball ZWT New Fine Pitch Ball Grid Array (Bottom View) – [Quadrant D]



A. Only the GPIO function is shown on GPIO pins. See [Table 4-1](#) for the complete, muxed signal name.

Figure 4-6. 100-Pin PZP PowerPAD HTQFP (Top View)

4.1 Signal Descriptions

Table 4-1 describes the signals. The GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. See Table 3-1 for details. All GPIO pins are I/O/Z and have an internal pullup, which can be selectively enabled or disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups are not enabled at reset.

Table 4-1. Signal Descriptions

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
ADC, DAC, AND COMPARATOR SIGNALS						
V _{REFHIA}		V1	37	19	I	ADC-A high reference. Place at least a 1-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode.
V _{REFHIB}		W5	53	37	I	ADC-B high reference. Place at least a 1-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode.
V _{REFHIC}		R1	35	–	I	ADC-C high reference. Place at least a 1-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode.
V _{REFHID}		V5	55	–	I	ADC-D high reference. Place at least a 1-μF capacitor on this pin for the 12-bit mode, or at least a 22-μF capacitor for the 16-bit mode.
V _{REFLOA}		R2	33	17	I	ADC-A low reference. On the PZP package, pin 17 is double-bonded to V _{SSA} and V _{REFLOA} . On the PZP package, pin 17 must be connected to V _{SSA} on the system board.
V _{REFLOB}		V6	50	34	I	ADC-B low reference
V _{REFLOC}		P2	32	–	I	ADC-C low reference
V _{REFLOD}		W6	51	–	I	ADC-D low reference
ADCIN14		T4	44	26	I	Input 14 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference.
CMPIN4P					I	Comparator 4 positive input
ADCIN15		U4	45	27	I	Input 15 to all ADCs. This pin can be used as a general-purpose ADCIN pin or it can be used to calibrate all ADCs together (either single-ended or differential) from an external reference.
CMPIN4N					I	Comparator 4 negative input
ADCINA0		U1	43	25	I	ADC-A input 0. There is a 50-kΩ pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTA					O	DAC-A output
ADCINA1		T1	42	24	I	ADC-A input 1. There is a 50-kΩ pulldown on this pin in both an ADC input or DAC output mode which cannot be disabled.
DACOUTB					O	DAC-B output
ADCINA2		U2	41	23	I	ADC-A input 2
CMPIN1P					I	Comparator 1 positive input
ADCINA3		T2	40	22	I	ADC-A input 3
CMPIN1N					I	Comparator 1 negative input
ADCINA4		U3	39	21	I	ADC-A input 4
CMPIN2P					I	Comparator 2 positive input

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
ADCINA5 CMPIN2N		T3	38	20	I I	ADC-A input 5 Comparator 2 negative input
ADCINB0 VDAC		V2	46	28	I I	ADC-B input 0 ⁽²⁾ Optional external reference voltage for on-chip DACs ⁽²⁾
ADCINB1 DACOUTC		W2	47	29	I O	ADC-B input 1. There is a 50-kΩ pull-down on this pin in both an ADC input or DAC output mode which cannot be disabled. DAC-C output
ADCINB2 CMPIN3P		V3	48	30	I I	ADC-B input 2 Comparator 3 positive input
ADCINB3 CMPIN3N		W3	49	31	I I	ADC-B input 3 Comparator 3 negative input
ADCINB4		V4	–	32	I	ADC-B input 4
ADCINB5		W4	–	33	I	ADC-B input 5
ADCINC2 CMPIN6P		R3	31	–	I I	ADC-C input 2 Comparator 6 positive input
ADCINC3 CMPIN6N		P3	30	–	I I	ADC-C input 3 Comparator 6 negative input
ADCINC4 CMPIN5P		R4	29	–	I I	ADC-C input 4 Comparator 5 positive input
ADCINC5 CMPIN5N		P4	–	–	I I	ADC-C input 5 Comparator 5 negative input
ADCIND0 CMPIN7P		T5	56	–	I I	ADC-D input 0 Comparator 7 positive input
ADCIND1 CMPIN7N		U5	57	–	I I	ADC-D input 1 Comparator 7 negative input
ADCIND2 CMPIN8P		T6	58	–	I I	ADC-D input 2 Comparator 8 positive input
ADCIND3 CMPIN8N		U6	59	–	I I	ADC-D input 3 Comparator 8 negative input
ADCIND4		T7	60	–	I	ADC-D input 4
ADCIND5		U7	–	–	I	ADC-D input 5
GPIO AND PERIPHERAL SIGNALS⁽³⁾						
GPIO0 EPWM1A SDAA	0, 4, 8, 12 1 6	C8	160	–	I/O O I/OD	General-purpose input/output 0 Enhanced PWM1 output A and HRPWM channel I2C-A data open-drain bidirectional port
GPIO1 EPWM1B MFSRB SCLA	0, 4, 8, 12 1 3 6	D8	161	–	I/O O I/O I/OD	General-purpose input/output 1 Enhanced PWM1 output B and HRPWM channel McBSP-B receive frame synch I2C-A clock open-drain bidirectional port
GPIO2 EPWM2A OUTPUTXBAR1 SDAB	0, 4, 8, 12 1 5 6	A7	162	91	I/O O O I/OD	General-purpose input/output 2 Enhanced PWM2 output A and HRPWM channel Output 1 of the output XBAR I2C-B data open-drain bidirectional port

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO3	0, 4, 8, 12				I/O	General-purpose input/output 3
EPWM2B	1				O	Enhanced PWM2 output B and HRPWM channel
OUTPUTXBAR2	2	B7	163	92	O	Output 2 of the output XBAR
MCLKRB	3				I/O	McBSP-B receive clock
OUTPUTXBAR2	5				O	Output 2 of the output XBAR
SCLB	6				I/OD	I2C-B clock open-drain bidirectional port
GPIO4	0, 4, 8, 12				I/O	General-purpose input/output 4
EPWM3A	1	C7	164	93	O	Enhanced PWM3 output A and HRPWM channel
OUTPUTXBAR3	5				O	Output 3 of the output XBAR
CANTXA	6				O	CAN-A transmit
GPIO5	0, 4, 8, 12				I/O	General-purpose input/output 5
EPWM3B	1				O	Enhanced PWM3 output B and HRPWM channel
MFSRA	2	D7	165	–	I/O	McBSP-A receive frame synch
OUTPUTXBAR3	3				O	Output 3 of the output XBAR
CANRXA	6				I	CAN-A receive
GPIO6	0, 4, 8, 12				I/O	General-purpose input/output 6
EPWM4A	1				O	Enhanced PWM4 output A and HRPWM channel
OUTPUTXBAR4	2	A6	166	–	O	Output 4 of the output XBAR
EPWMSYNCO	3				O	External ePWM synch pulse output
EQEP3A	5				I	Enhanced QEP3 input A
CANTXB	6				O	CAN-B transmit
GPIO7	0, 4, 8, 12				I/O	General-purpose input/output 7
EPWM4B	1				O	Enhanced PWM4 output B and HRPWM channel
MCLKRA	2	B6	167	–	I/O	McBSP-A receive clock
OUTPUTXBAR5	3				O	Output 5 of the output XBAR
EQEP3B	5				I	Enhanced QEP3 input B
CANRXB	6				I	CAN-B receive
GPIO8	0, 4, 8, 12				I/O	General-purpose input/output 8
EPWM5A	1				O	Enhanced PWM5 output A and HRPWM channel
CANTXB	2	G2	18	–	O	CAN-B transmit
ADCSOCAO	3				O	ADC start-of-conversion A
EQEP3S	5				I/O	Enhanced QEP3 strobe
SCITXDA	6				O	SCI-A transmit data
GPIO9	0, 4, 8, 12				I/O	General-purpose input/output 9
EPWM5B	1				O	Enhanced PWM5 output B and HRPWM channel
SCITXDB	2	G3	19	–	O	SCI-B transmit data
OUTPUTXBAR6	3				O	Output 6 of the output XBAR
EQEP3I	5				I/O	Enhanced QEP3 index
SCIRXDA	6				I	SCI-A receive data

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO10	0, 4, 8, 12				I/O	General-purpose input/output 10
EPWM6A	1				O	Enhanced PWM6 output A and HRPWM channel
CANRXB	2				I	CAN-B receive
ADCSOCBO	3	B2	1	100	O	ADC start-of-conversion B
EQEP1A	5				I	Enhanced QEP1 input A
SCITXDB	6				O	SCI-B transmit data
UPP-WAIT	15				I/O	Universal parallel port wait. Receiver asserts to request a pause in transfer.
GPIO11	0, 4, 8, 12				I/O	General-purpose input/output 11
EPWM6B	1				O	Enhanced PWM6 output B and HRPWM channel
SCIRXDB	2, 6				I	SCI-B receive data
OUTPUTXBAR7	3	C1	2	1	O	Output 7 of the output XBAR
EQEP1B	5				I	Enhanced QEP1 input B
UPP-STRT	15				I/O	Universal parallel port start. Transmitter asserts at start of DMA line.
GPIO12	0, 4, 8, 12				I/O	General-purpose input/output 12
EPWM7A	1				O	Enhanced PWM7 output A and HRPWM channel
CANTXB	2				O	CAN-B transmit
MDXB	3	C2	4	3	O	McBSP-B transmit serial data
EQEP1S	5				I/O	Enhanced QEP1 strobe
SCITXDC	6				O	SCI-C transmit data
UPP-ENA	15				I/O	Universal parallel port enable. Transmitter asserts while data bus is active.
GPIO13	0, 4, 8, 12				I/O	General-purpose input/output 13
EPWM7B	1				O	Enhanced PWM7 output B and HRPWM channel
CANRXB	2				I	CAN-B receive
MDRB	3	D1	5	4	I	McBSP-B receive serial data
EQEP1I	5				I/O	Enhanced QEP1 index
SCIRXDC	6				I	SCI-C receive data
UPP-D7	15				I/O	Universal parallel port data line 7
GPIO14	0, 4, 8, 12				I/O	General-purpose input/output 14
EPWM8A	1				O	Enhanced PWM8 output A and HRPWM channel
SCITXDB	2	D2	6	5	O	SCI-B transmit data
MCLKXB	3				I/O	McBSP-B transmit clock
OUTPUTXBAR3	6				O	Output 3 of the output XBAR
UPP-D6	15				I/O	Universal parallel port data line 6
GPIO15	0, 4, 8, 12				I/O	General-purpose input/output 15
EPWM8B	1				O	Enhanced PWM8 output B and HRPWM channel
SCIRXDB	2	D3	7	6	I	SCI-B receive data
MFSXB	3				I/O	McBSP-B transmit frame synch
OUTPUTXBAR4	6				O	Output 4 of the output XBAR
UPP-D5	15				I/O	Universal parallel port data line 5

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO16	0, 4, 8, 12				I/O	General-purpose input/output 16
SPISIMOA	1				I/O	SPI-A slave in, master out
CANTXB	2				O	CAN-B transmit
OUTPUTXBAR7	3	E1	8	7	O	Output 7 of the output XBAR
EPWM9A	5				O	Enhanced PWM9 output A
SD1_D1	7				I	Sigma-Delta 1 channel 1 data input
UPP-D4	15				I/O	Universal parallel port data line 4
GPIO17	0, 4, 8, 12				I/O	General-purpose input/output 17
SPISOMIA	1				I/O	SPI-A slave out, master in
CANRXB	2				I	CAN-B receive
OUTPUTXBAR8	3	E2	9	8	O	Output 8 of the output XBAR
EPWM9B	5				O	Enhanced PWM9 output B
SD1_C1	7				I	Sigma-Delta 1 channel 1 clock input
UPP-D3	15				I/O	Universal parallel port data line 3
GPIO18	0, 4, 8, 12				I/O	General-purpose input/output 18
SPICLKA	1				I/O	SPI-A clock
SCITXDB	2				O	SCI-B transmit data
CANRXA	3	E3	10	9	I	CAN-A receive
EPWM10A	5				O	Enhanced PWM10 output A
SD1_D2	7				I	Sigma-Delta 1 channel 2 data input
UPP-D2	15				I/O	Universal parallel port data line 2
GPIO19	0, 4, 8, 12				I/O	General-purpose input/output 19
SPISTEA	1				I/O	SPI-A slave transmit enable
SCIRXDB	2				I	SCI-B receive data
CANTXA	3	E4	12	11	O	CAN-A transmit
EPWM10B	5				O	Enhanced PWM10 output B
SD1_C2	7				I	Sigma-Delta 1 channel 2 clock input
UPP-D1	15				I/O	Universal parallel port data line 1
GPIO20	0, 4, 8, 12				I/O	General-purpose input/output 20
EQEP1A	1				I	Enhanced QEP1 input A
MDXA	2				O	McBSP-A transmit serial data
CANTXB	3	F2	13	12	O	CAN-B transmit
EPWM11A	5				O	Enhanced PWM11 output A
SD1_D3	7				I	Sigma-Delta 1 channel 3 data input
UPP-D0	15				I/O	Universal parallel port data line 0
GPIO21	0, 4, 8, 12				I/O	General-purpose input/output 21
EQEP1B	1				I	Enhanced QEP1 input B
MDRA	2				I	McBSP-A receive serial data
CANRXB	3	F3	14	13	I	CAN-B receive
EPWM11B	5				O	Enhanced PWM11 output B
SD1_C3	7				I	Sigma-Delta 1 channel 3 clock input
UPP-CLK	15				I/O	Universal parallel port transmit clock

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO22	0, 2, 4, 8				I/O	General-purpose input/output 22
EQEP1S	1				I/O	Enhanced QEP1 strobe
MCLKXA	2				I/O	McBSP-A transmit clock
SCITXDB	3	J4	22	–	O	SCI-B transmit data
EPWM12A	5				O	Enhanced PWM12 output A
SPICKB	6				I/O	SPI-B clock
SD1_D4	7				I	Sigma-Delta 1 channel 4 data input
GPIO23	0, 2, 4, 8				I/O	General-purpose input/output 23
EQEP1I	1				I/O	Enhanced QEP1 index
MFSXA	2				I/O	McBSP-A transmit frame synch
SCIRXDB	3	K4	23	–	I	SCI-B receive data
EPWM12B	5				O	Enhanced PWM12 output B
$\overline{\text{SPISTEB}}$	6				I/O	SPI-B slave transmit enable
SD1_C4	7				I	Sigma-Delta 1 channel 4 clock input
GPIO24	0, 4, 8, 12				I/O	General-purpose input/output 24
OUTPUTXBAR1	1				O	Output 1 of the output XBAR
EQEP2A	2	K3	24	–	I	Enhanced QEP2 input A
MDXB	3				O	McBSP-B transmit serial data
SPISIMOB	6				I/O	SPI-B slave in, master out
SD2_D1	7				I	Sigma-Delta 2 channel 1 data input
GPIO25	0, 4, 8, 12				I/O	General-purpose input/output 25
OUTPUTXBAR2	1				O	Output 2 of the output XBAR
EQEP2B	2	K2	25	–	I	Enhanced QEP2 input B
MDRB	3				I	McBSP-B receive serial data
SPISOMIB	6				I/O	SPI-B slave out, master in
SD2_C1	7				I	Sigma-Delta 2 channel 1 clock input
GPIO26	0, 4, 8, 12				I/O	General-purpose input/output 26
OUTPUTXBAR3	1				O	Output 3 of the output XBAR
EQEP2I	2				I/O	Enhanced QEP2 index
MCLKXB	3	K1	27	–	I/O	McBSP-B transmit clock
OUTPUTXBAR3	5				O	Output 3 of the output XBAR
SPICKB	6				I/O	SPI-B clock
SD2_D2	7				I	Sigma-Delta 2 channel 2 data input
GPIO27	0, 4, 8, 12				I/O	General-purpose input/output 27
OUTPUTXBAR4	1				O	Output 4 of the output XBAR
EQEP2S	2				I/O	Enhanced QEP2 strobe
MFSXB	3	L1	28	–	I/O	McBSP-B transmit frame synch
OUTPUTXBAR4	5				O	Output 4 of the output XBAR
$\overline{\text{SPISTEB}}$	6				I/O	SPI-B slave transmit enable
SD2_C2	7				I	Sigma-Delta 2 channel 2 clock input

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO28	0, 4, 8, 12	V11	64	-	I/O	General-purpose input/output 28
SCIRXDA	1				I	SCI-A receive data
EM1CS4	2				O	External memory interface 1 chip select 4
OUTPUTXBAR5	5				O	Output 5 of the output XBAR
EQEP3A	6				I	Enhanced QEP3 input A
SD2_D3	7				I	Sigma-Delta 2 channel 3 data input
GPIO29	0, 4, 8, 12				W11	65
SCITXDA	1	O	SCI-A transmit data			
EM1SDCKE	2	O	External memory interface 1 SDRAM clock enable			
OUTPUTXBAR6	5	O	Output 6 of the output XBAR			
EQEP3B	6	I	Enhanced QEP3 input B			
SD2_C3	7	I	Sigma-Delta 2 channel 3 clock input			
GPIO30	0, 4, 8, 12	T11	63	-	I/O	General-purpose input/output 30
CANRXA	1				I	CAN-A receive
EM1CLK	2				O	External memory interface 1 clock
OUTPUTXBAR7	5				O	Output 7 of the output XBAR
EQEP3S	6				I/O	Enhanced QEP3 strobe
SD2_D4	7				I	Sigma-Delta 2 channel 4 data input
GPIO31	0, 4, 8, 12	U11	66	-	I/O	General-purpose input/output 31
CANTXA	1				O	CAN-A transmit
EM1WE	2				O	External memory interface1 write enable
OUTPUTXBAR8	5				O	Output 8 of the output XBAR
EQEP3I	6				I/O	Enhanced QEP3 index
SD2_C4	7				I	Sigma-Delta 2 channel 4 clock input
GPIO32	0, 4, 8, 12	U13	67	-	I/O	General-purpose input/output 32
SDAA	1				I/OD	I2C-A data open-drain bidirectional port
EM1CS0	2				O	External memory interface 1 chip select 0
GPIO33	0, 4, 8, 12	T13	69	-	I/O	General-purpose input/output 33
SCLA	1				I/OD	I2C-A clock open-drain bidirectional port
EM1RNW	2				O	External memory interface 1 read not write
GPIO34	0, 4, 8, 12	U14	70	-	I/O	General-purpose input/output 34
OUTPUTXBAR1	1				O	Output 1 of the output XBAR
EM1CS2	2				O	External memory interface 1 chip select 2
SDAB	6				I/OD	I2C-B data open-drain bidirectional port
GPIO35	0, 4, 8, 12	T14	71	-	I/O	General-purpose input/output 35
SCIRXDA	1				I	SCI-A receive data
EM1CS3	2				O	External memory interface 1 chip select 3
SCLB	6				I/OD	I2C-B clock open-drain bidirectional port
GPIO36	0, 4, 8, 12	V16	83	-	I/O	General-purpose input/output 36
SCITXDA	1				O	SCI-A transmit data
EM1WAIT	2				I	External memory interface 1 Asynchronous SRAM WAIT
CANRXA	6				I	CAN-A receive

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO37	0, 4, 8, 12				I/O	General-purpose input/output 37
OUTPUTXBAR2	1	U16	84	–	O	Output 2 of the output XBAR
EM1OE	2				O	External memory interface 1 output enable
CANTXA	6				O	CAN-A transmit
GPIO38	0, 4, 8, 12				I/O	General-purpose input/output 38
EM1A0	2	T16	85	–	O	External memory interface 1 address line 0
SCITXDC	5				O	SCI-C transmit data
CANTXB	6				O	CAN-B transmit
GPIO39	0, 4, 8, 12				I/O	General-purpose input/output 39
EM1A1	2	W17	86	–	O	External memory interface 1 address line 1
SCIRXDC	5				I	SCI-C receive data
CANRXB	6				I	CAN-B receive
GPIO40	0, 4, 8, 12				I/O	General-purpose input/output 40
EM1A2	2	V17	87	–	O	External memory interface 1 address line 2
SDAB	6				I/OD	I2C-B data open-drain bidirectional port
GPIO41	0, 4, 8, 12				I/O	General-purpose input/output 41
EM1A3	2	U17	89	51	O	External memory interface 1 address line 3
SCLB	6				I/OD	I2C-B clock open-drain bidirectional port
GPIO42	0, 4, 8, 12				I/O	General-purpose input/output 42
SDAA	6	D19	130	73	I/OD	I2C-A data open-drain bidirectional port
SCITXDA	15				O	SCI-A transmit data
USB0DM	Analog				I/O	USB PHY differential data
GPIO43	0, 4, 8, 12				I/O	General-purpose input/output 43
SCLA	6	C19	131	74	I/OD	I2C-A clock open-drain bidirectional port
SCIRXDA	15				I	SCI-A receive data
USB0DP	Analog				I/O	USB PHY differential data
GPIO44	0, 4, 8, 12				I/O	General-purpose input/output 44
EM1A4	2	K18	113	–	O	External memory interface 1 address line 4
GPIO45	0, 4, 8, 12				I/O	General-purpose input/output 45
EM1A5	2	K19	115	–	O	External memory interface 1 address line 5
GPIO46	0, 4, 8, 12				I/O	General-purpose input/output 46
EM1A6	2	E19	128	–	O	External memory interface 1 address line 6
SCIRXDD	6				I	SCI-D receive data
GPIO47	0, 4, 8, 12				I/O	General-purpose input/output 47
EM1A7	2	E18	129	–	O	External memory interface 1 address line 7
SCITXDD	6				O	SCI-D transmit data
GPIO48	0, 4, 8, 12				I/O	General-purpose input/output 48
OUTPUTXBAR3	1	R16	90	–	O	Output 3 of the output XBAR
EM1A8	2				O	External memory interface 1 address line 8
SCITXDA	6				O	SCI-A transmit data
SD1_D1	7				I	Sigma-Delta 1 channel 1 data input

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO49	0, 4, 8, 12				I/O	General-purpose input/output 49
OUTPUTXBAR4	1				O	Output 4 of the output XBAR
EM1A9	2	R17	93	–	O	External memory interface 1 address line 9
SCIRXDA	6				I	SCI-A receive data
SD1_C1	7				I	Sigma-Delta 1 channel 1 clock input
GPIO50	0, 4, 8, 12				I/O	General-purpose input/output 50
EQEP1A	1				I	Enhanced QEP1 input A
EM1A10	2	R18	94	–	O	External memory interface 1 address line 10
SPISIMOC	6				I/O	SPI-C slave in, master out
SD1_D2	7				I	Sigma-Delta 1 channel 2 data input
GPIO51	0, 4, 8, 12				I/O	General-purpose input/output 51
EQEP1B	1				I	Enhanced QEP1 input B
EM1A11	2	R19	95	–	O	External memory interface 1 address line 11
SPISOMIC	6				I/O	SPI-C slave out, master in
SD1_C2	7				I	Sigma-Delta 1 channel 2 clock input
GPIO52	0, 4, 8, 12				I/O	General-purpose input/output 52
EQEP1S	1				I/O	Enhanced QEP1 strobe
EM1A12	2	P16	96	–	O	External memory interface 1 address line 12
SPICKKC	6				I/O	SPI-C clock
SD1_D3	7				I	Sigma-Delta 1 channel 3 data input
GPIO53	0, 4, 8, 12				I/O	General-purpose input/output 53
EQEP1I	1				I/O	Enhanced QEP1 index
EM1D31	2	P17	97	–	I/O	External memory interface 1 data line 31
EM2D15	3				I/O	External memory interface 2 data line 15
SPISTEC	6				I/O	SPI-C slave transmit enable
SD1_C3	7				I	Sigma-Delta 1 channel 3 clock input
GPIO54	0, 4, 8, 12				I/O	General-purpose input/output 54
SPISIMOA	1				I/O	SPI-A slave in, master out
EM1D30	2	P18	98	–	I/O	External memory interface 1 data line 30
EM2D14	3				I/O	External memory interface 2 data line 14
EQEP2A	5				I	Enhanced QEP2 input A
SCITXDB	6				O	SCI-B transmit data
SD1_D4	7				I	Sigma-Delta 1 channel 4 data input
GPIO55	0, 4, 8, 12				I/O	General-purpose input/output 55
SPISOMIA	1				I/O	SPI-A slave out, master in
EM1D29	2	P19	100	–	I/O	External memory interface 1 data line 29
EM2D13	3				I/O	External memory interface 2 data line 13
EQEP2B	5				I	Enhanced QEP2 input B
SCIRXDB	6				I	SCI-B receive data
SD1_C4	7				I	Sigma-Delta 1 channel 4 clock input

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO56	0, 4, 8, 12				I/O	General-purpose input/output 56
SPICLKA	1				I/O	SPI-A clock
EM1D28	2				I/O	External memory interface 1 data line 28
EM2D12	3	N16	101	–	I/O	External memory interface 2 data line 12
EQEP2S	5				I/O	Enhanced QEP2 strobe
SCITXDC	6				O	SCI-C transmit data
SD2_D1	7				I	Sigma-Delta 2 channel 1 data input
GPIO57	0, 4, 8, 12				I/O	General-purpose input/output 57
$\overline{\text{SPISTEA}}$	1				I/O	SPI-A slave transmit enable
EM1D27	2				I/O	External memory interface 1 data line 27
EM2D11	3	N18	102	–	I/O	External memory interface 2 data line 11
EQEP2I	5				I/O	Enhanced QEP2 index
SCIRXDC	6				I	SCI-C receive data
SD2_C1	7				I	Sigma-Delta 2 channel 1 clock input
GPIO58	0, 4, 8, 12				I/O	General-purpose input/output 58
MCLKRA	1				I/O	McBSP-A receive clock
EM1D26	2				I/O	External memory interface 1 data line 26
EM2D10	3				I/O	External memory interface 2 data line 10
OUTPUTXBAR1	5	N17	103	52	O	Output 1 of the output XBAR
SPICLKB	6				I/O	SPI-B clock
SD2_D2	7				I	Sigma-Delta 2 channel 2 data input
SPISIMOA	15				I/O	SPI-A slave in, master out ⁽⁴⁾
GPIO59	0, 4, 8, 12				I/O	General-purpose input/output 59 ⁽⁵⁾
MFSRA	1				I/O	McBSP-A receive frame synch
EM1D25	2				I/O	External memory interface 1 data line 25
EM2D9	3				I/O	External memory interface 2 data line 9
OUTPUTXBAR2	5	M16	104	53	O	Output 2 of the output XBAR
$\overline{\text{SPISTEB}}$	6				I/O	SPI-B slave transmit enable
SD2_C2	7				I	Sigma-Delta 2 channel 2 clock input
SPISOMIA	15				I/O	SPI-A slave out, master in ⁽⁴⁾
GPIO60	0, 4, 8, 12				I/O	General-purpose input/output 60
MCLKRB	1				I/O	McBSP-B receive clock
EM1D24	2				I/O	External memory interface 1 data line 24
EM2D8	3				I/O	External memory interface 2 data line 8
OUTPUTXBAR3	5	M17	105	54	O	Output 3 of the output XBAR
SPISIMOB	6				I/O	SPI-B slave in, master out
SD2_D3	7				I	Sigma-Delta 2 channel 3 data input
SPICLKA	15				I/O	SPI-A clock ⁽⁴⁾

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO61	0, 4, 8, 12	L16	107	56	I/O	General-purpose input/output 61 ⁽⁵⁾
MFSRB	1				I/O	McBSP-B receive frame synch
EM1D23	2				I/O	External memory interface 1 data line 23
EM2D7	3				I/O	External memory interface 2 data line 7
OUTPUTXBAR4	5				O	Output 4 of the output XBAR
SPISOMIB	6				I/O	SPI-B slave out, master in
SD2_C3	7				I	Sigma-Delta 2 channel 3 clock input
SPISTEA	15				I/O	SPI-A slave transmit enable ⁽⁴⁾
GPIO62	0, 4, 8, 12	J17	108	57	I/O	General-purpose input/output 62
SCIRXDC	1				I	SCI-C receive data
EM1D22	2				I/O	External memory interface 1 data line 22
EM2D6	3				I/O	External memory interface 2 data line 6
EQEP3A	5				I	Enhanced QEP3 input A
CANRXA	6				I	CAN-A receive
SD2_D4	7				I	Sigma-Delta 2 channel 4 data input
GPIO63	0, 4, 8, 12	J16	109	58	I/O	General-purpose input/output 63
SCITXDC	1				O	SCI-C transmit data
EM1D21	2				I/O	External memory interface 1 data line 21
EM2D5	3				I/O	External memory interface 2 data line 5
EQEP3B	5				I	Enhanced QEP3 input B
CANTXA	6				O	CAN-A transmit
SD2_C4	7				I	Sigma-Delta 2 channel 4 clock input
SPISIMOB	15				I/O	SPI-B slave in, master out ⁽⁴⁾
GPIO64	0, 4, 8, 12	L17	110	59	I/O	General-purpose input/output 64 ⁽⁵⁾
EM1D20	2				I/O	External memory interface 1 data line 20
EM2D4	3				I/O	External memory interface 2 data line 4
EQEP3S	5				I/O	Enhanced QEP3 strobe
SCIRXDA	6				I	SCI-A receive data
SPISOMIB	15				I/O	SPI-B slave out, master in ⁽⁴⁾
GPIO65	0, 4, 8, 12				K16	111
EM1D19	2	I/O	External memory interface 1 data line 19			
EM2D3	3	I/O	External memory interface 2 data line 3			
EQEP3I	5	I/O	Enhanced QEP3 index			
SCITXDA	6	O	SCI-A transmit data			
SPICLKB	15	I/O	SPI-B clock ⁽⁴⁾			
GPIO66	0, 4, 8, 12	K17	112	61	I/O	General-purpose input/output 66 ⁽⁵⁾
EM1D18	2				I/O	External memory interface 1 data line 18
EM2D2	3				I/O	External memory interface 2 data line 2
SDAB	6				I/OD	I2C-B data open-drain bidirectional port
SPISTEB	15				I/O	SPI-B slave transmit enable ⁽⁴⁾
GPIO67	0, 4, 8, 12	B19	132	–	I/O	General-purpose input/output 67
EM1D17	2				I/O	External memory interface 1 data line 17
EM2D1	3				I/O	External memory interface 2 data line 1

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO68	0, 4, 8, 12				I/O	General-purpose input/output 68
EM1D16	2	C18	133	–	I/O	External memory interface 1 data line 16
EM2D0	3				I/O	External memory interface 2 data line 0
GPIO69	0, 4, 8, 12				I/O	General-purpose input/output 69
EM1D15	2	B18	134	75	I/O	External memory interface 1 data line 15
SCLB	6				I/OD	I2C-B clock open-drain bidirectional port
SPISIMOC	15				I/O	SPI-C slave in, master out ⁽⁴⁾
GPIO70	0, 4, 8, 12				I/O	General-purpose input/output 70 ⁽⁵⁾
EM1D14	2				I/O	External memory interface 1 data line 14
CANRXA	5	A17	135	76	I	CAN-A receive
SCITXDB	6				O	SCI-B transmit data
SPISOMIC	15				I/O	SPI-C slave out, master in ⁽⁴⁾
GPIO71	0, 4, 8, 12				I/O	General-purpose input/output 71
EM1D13	2				I/O	External memory interface 1 data line 13
CANTXA	5	B17	136	77	O	CAN-A transmit
SCIRXDB	6				I	SCI-B receive data
SPICLK	15				I/O	SPI-C clock ⁽⁴⁾
GPIO72	0, 4, 8, 12				I/O	General-purpose input/output 72 ⁽⁵⁾
EM1D12	2				I/O	External memory interface 1 data line 12
CANTXB	5	B16	139	80	O	CAN-B transmit
SCITXDC	6				O	SCI-C transmit data
SPISTEC	15				I/O	SPI-C slave transmit enable ⁽⁴⁾
GPIO73	0, 4, 8, 12				I/O	General-purpose input/output 73
EM1D11	2				I/O	External memory interface 1 data line 11
XCLKOUT	3				O/Z	External clock output. This pin outputs a divided-down version of a chosen clock signal from within the device. The clock signal is chosen using the CLKSRCTL3.XCLKOUTSEL bit field while the divide ratio is chosen using the XCLKOUTDIVSEL.XCLKOUTDIV bit field. Unlike other GPIO pins, the XCLKOUT pin is not placed in high-impedance state during a reset.
CANRXB	5	A16	140	81	I	CAN-B receive
SCIRXDC	6				I	SCI-C receive
GPIO74	0, 4, 8, 12				I/O	General-purpose input/output 74
EM1D10	2	C17	141	–	I/O	External memory interface 1 data line 10
GPIO75	0, 4, 8, 12				I/O	General-purpose input/output 75
EM1D9	2	D16	142	–	I/O	External memory interface 1 data line 9
GPIO76	0, 4, 8, 12				I/O	General-purpose input/output 76
EM1D8	2	C16	143	–	I/O	External memory interface 1 data line 8
SCITXDD	6				O	SCI-D transmit data
GPIO77	0, 4, 8, 12				I/O	General-purpose input/output 77
EM1D7	2	A15	144	–	I/O	External memory interface 1 data line 7
SCIRXDD	6				I	SCI-D receive data
GPIO78	0, 4, 8, 12				I/O	General-purpose input/output 78
EM1D6	2	B15	145	82	I/O	External memory interface 1 data line 6
EQEP2A	6				I	Enhanced QEP2 input A

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO79	0, 4, 8, 12				I/O	General-purpose input/output 79
EM1D5	2	C15	146	–	I/O	External memory interface 1 data line 5
EQEP2B	6				I	Enhanced QEP2 input B
GPIO80	0, 4, 8, 12				I/O	General-purpose input/output 80
EM1D4	2	D15	148	–	I/O	External memory interface 1 data line 4
EQEP2S	6				I/O	Enhanced QEP2 strobe
GPIO81	0, 4, 8, 12				I/O	General-purpose input/output 81
EM1D3	2	A14	149	–	I/O	External memory interface 1 data line 3
EQEP2I	6				I/O	Enhanced QEP2 index
GPIO82	0, 4, 8, 12				I/O	General-purpose input/output 82
EM1D2	2	B14	150	–	I/O	External memory interface 1 data line 2
GPIO83	0, 4, 8, 12				I/O	General-purpose input/output 83
EM1D1	2	C14	151	–	I/O	External memory interface 1 data line 1
GPIO84	0, 4, 8, 12				I/O	General-purpose input/output 84
SCITXDA	5	A11	154	85	O	SCI-A transmit data
MDXB	6				O	McBSP-B transmit serial data
MDXA	15				O	McBSP-A transmit serial data
GPIO85	0, 4, 8, 12				I/O	General-purpose input/output 85
EM1D0	2				I/O	External memory interface 1 data line 0
SCIRXDA	5	B11	155	86	I	SCI-A receive data
MDRB	6				I	McBSP-B receive serial data
MDRA	15				I	McBSP-A receive serial data
GPIO86	0, 4, 8, 12				I/O	General-purpose input/output 86
EM1A13	2				O	External memory interface 1 address line 13
EM1CAS	3	C11	156	87	O	External memory interface 1 column address strobe
SCITXDB	5				O	SCI-B transmit data
MCLKXB	6				I/O	McBSP-B transmit clock
MCLKXA	15				I/O	McBSP-A transmit clock
GPIO87	0, 2, 4, 8				I/O	General-purpose input/output 87
EM1A14	2				O	External memory interface 1 address line 14
EM1RAS	3	D11	157	88	O	External memory interface 1 row address strobe
SCIRXDB	5				I	SCI-B receive data
MFSXB	6				I/O	McBSP-B transmit frame synch
MFSXA	15				I/O	McBSP-A transmit frame synch
GPIO88	0, 2, 4, 8				I/O	General-purpose input/output 88
EM1A15	2	C6	170	–	O	External memory interface 1 address line 15
EM1DQM0	3				O	External memory interface 1 Input/output mask for byte 0
GPIO89	0, 2, 4, 8				I/O	General-purpose input/output 89
EM1A16	2	D6	171	96	O	External memory interface 1 address line 16
EM1DQM1	3				O	External memory interface 1 Input/output mask for byte 1
SCITXDC	6				O	SCI-C transmit data
GPIO90	0, 2, 4, 8				I/O	General-purpose input/output 90
EM1A17	2	A5	172	97	O	External memory interface 1 address line 17
EM1DQM2	3				O	External memory interface 1 Input/output mask for byte 2
SCIRXDC	6				I	SCI-C receive data

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO91	0, 2, 4, 8				I/O	General-purpose input/output 91
EM1A18	2	B5	173	98	O	External memory interface 1 address line 18
EM1DQM3	3				O	External memory interface 1 Input/output mask for byte 3
SDAA	6				I/OD	I2C-A data open-drain bidirectional port
GPIO92	0, 2, 4, 8				I/O	General-purpose input/output 92
EM1A19	2	A4	174	99	O	External memory interface 1 address line 19
EM1BA1	3				O	External memory interface 1 bank address 1
SCLA	6				I/OD	I2C-A clock open-drain bidirectional port
GPIO93	0, 2, 4, 8				I/O	General-purpose input/output 93
EM1BA0	3	B4	175	–	O	External memory interface 1 bank address 0
SCITXDD	6				O	SCI-D transmit data
GPIO94	0, 2, 4, 8				I/O	General-purpose input/output 94
SCIRXDD	6	A3	176	–	I	SCI-D receive data
GPIO95	0, 2, 4, 8	B3	–	–	I/O	General-purpose input/output 95
GPIO96	0, 2, 4, 8				I/O	General-purpose input/output 96
EM2DQM1	3	C3	–	–	O	External memory interface 2 Input/output mask for byte 1
EQEP1A	5				I	Enhanced QEP1 input A
GPIO97	0, 2, 4, 8				I/O	General-purpose input/output 97
EM2DQM0	3	A2	–	–	O	External memory interface 2 Input/output mask for byte 0
EQEP1B	5				I	Enhanced QEP1 input B
GPIO98	0, 2, 4, 8				I/O	General-purpose input/output 98
EM2A0	3	F1	–	–	O	External memory interface 2 address line 0
EQEP1S	5				I/O	Enhanced QEP1 strobe
GPIO99	0, 2, 4, 8				I/O	General-purpose input/output 99
EM2A1	3	G1	17	14	O	External memory interface 2 address line 1
EQEP1I	5				I/O	Enhanced QEP1 index
GPIO100	0, 4, 8, 12				I/O	General-purpose input/output 100
EM2A2	3	H1	–	–	O	External memory interface 2 address line 2
EQEP2A	5				I	Enhanced QEP2 input A
SPISIMOC	6				I/O	SPI-C slave in, master out
GPIO101	0, 4, 8, 12				I/O	General-purpose input/output 101
EM2A3	3	H2	–	–	O	External memory interface 2 address line 3
EQEP2B	5				I	Enhanced QEP2 input B
SPISOMIC	6				I/O	SPI-C slave out, master in
GPIO102	0, 4, 8, 12				I/O	General-purpose input/output 102
EM2A4	3	H3	–	–	O	External memory interface 2 address line 4
EQEP2S	5				I/O	Enhanced QEP2 strobe
SPICLK	6				I/O	SPI-C clock
GPIO103	0, 4, 8, 12				I/O	General-purpose input/output 103
EM2A5	3	J1	–	–	O	External memory interface 2 address line 5
EQEP2I	5				I/O	Enhanced QEP2 index
SPISTEC	6				I/O	SPI-C slave transmit enable

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO104	0, 4, 8, 12				I/O	General-purpose input/output 104
SDAA	1				I/OD	I2C-A data open-drain bidirectional port
EM2A6	3	J2	–	–	O	External memory interface 2 address line 6
EQEP3A	5				I	Enhanced QEP3 input A
SCITXDD	6				O	SCI-D transmit data
GPIO105	0, 4, 8, 12				I/O	General-purpose input/output 105
SCLA	1				I/OD	I2C-A clock open-drain bidirectional port
EM2A7	3	J3	–	–	O	External memory interface 2 address line 7
EQEP3B	5				I	Enhanced QEP3 input B
SCIRXDD	6				I	SCI-D receive data
GPIO106	0, 4, 8, 12				I/O	General-purpose input/output 106
EM2A8	3	L2	–	–	O	External memory interface 2 address line 8
EQEP3S	5				I/O	Enhanced QEP3 strobe
SCITXDC	6				O	SCI-C transmit data
GPIO107	0, 4, 8, 12				I/O	General-purpose input/output 107
EM2A9	3	L3	–	–	O	External memory interface 2 address line 9
EQEP3I	5				I/O	Enhanced QEP3 index
SCIRXDC	6				I	SCI-C receive data
GPIO108	0, 4, 8, 12				I/O	General-purpose input/output 108
EM2A10	3	L4	–	–	O	External memory interface 2 address line 10
GPIO109	0, 4, 8, 12				I/O	General-purpose input/output 109
EM2A11	3	N2	–	–	O	External memory interface 2 address line 11
GPIO110	0, 4, 8, 12				I/O	General-purpose input/output 110
EM2WAIT	3	M2	–	–	I	External memory interface 2 Asynchronous SRAM WAIT
GPIO111	0, 4, 8, 12				I/O	General-purpose input/output 111
EM2BA0	3	M4	–	–	O	External memory interface 2 bank address 0
GPIO112	0, 4, 8, 12				I/O	General-purpose input/output 112
EM2BA1	3	M3	–	–	O	External memory interface 2 bank address 1
GPIO113	0, 4, 8, 12				I/O	General-purpose input/output 113
EM2CAS	3	N4	–	–	O	External memory interface 2 column address strobe
GPIO114	0, 4, 8, 12				I/O	General-purpose input/output 114
EM2RAS	3	N3	–	–	O	External memory interface 2 row address strobe
GPIO115	0, 4, 8, 12				I/O	General-purpose input/output 115
EM2CS0	3	V12	–	–	O	External memory interface 2 chip select 0
GPIO116	0, 4, 8, 12				I/O	General-purpose input/output 116
EM2CS2	3	W10	–	–	O	External memory interface 2 chip select 2
GPIO117	0, 4, 8, 12				I/O	General-purpose input/output 117
EM2SDCKE	3	U12	–	–	O	External memory interface 2 SDRAM clock enable
GPIO118	0, 4, 8, 12				I/O	General-purpose input/output 118
EM2CLK	3	T12	–	–	O	External memory interface 2 clock
GPIO119	0, 4, 8, 12				I/O	General-purpose input/output 119
EM2RNW	3	T15	–	–	O	External memory interface 2 read not write
GPIO120	0, 4, 8, 12				I/O	General-purpose input/output 120
EM2WE	3	U15	–	–	O	External memory interface 2 write enable
USB0PFLT	15				I/O	USB external regulator power fault indicator

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO121	0, 4, 8, 12				I/O	General-purpose input/output 121
$\overline{\text{EM2OE}}$	3	W16	–	–	O	External memory interface 2 output enable
USB0EPEN	15				I/O	USB external regulator enable
GPIO122	0, 4, 8, 12				I/O	General-purpose input/output 122
SPISIMOC	6	T8	–	–	I/O	SPI-C slave in, master out
SD1_D1	7				I	Sigma-Delta 1 channel 1 data input
GPIO123	0, 4, 8, 12				I/O	General-purpose input/output 123
SPISOMIC	6	U8	–	–	I/O	SPI-C slave out, master in
SD1_C1	7				I	Sigma-Delta 1 channel 1 clock input
GPIO124	0, 4, 8, 12				I/O	General-purpose input/output 124
SPICLK	6	V8	–	–	I/O	SPI-C clock
SD1_D2	7				I	Sigma-Delta 1 channel 2 data input
GPIO125	0, 4, 8, 12				I/O	General-purpose input/output 125
$\overline{\text{SPISTEC}}$	6	T9	–	–	I/O	SPI-C slave transmit enable
SD1_C2	7				I	Sigma-Delta 1 channel 2 clock input
GPIO126	0, 4, 8, 12				I/O	General-purpose input/output 126
SD1_D3	7	U9	–	–	I	Sigma-Delta 1 channel 3 data input
GPIO127	0, 4, 8, 12				I/O	General-purpose input/output 127
SD1_C3	7	V9	–	–	I	Sigma-Delta 1 channel 3 clock input
GPIO128	0, 4, 8, 12				I/O	General-purpose input/output 128
SD1_D4	7	W9	–	–	I	Sigma-Delta 1 channel 4 data input
GPIO129	0, 4, 8, 12				I/O	General-purpose input/output 129
SD1_C4	7	T10	–	–	I	Sigma-Delta 1 channel 4 clock input
GPIO130	0, 4, 8, 12				I/O	General-purpose input/output 130
SD2_D1	7	U10	–	–	I	Sigma-Delta 2 channel 1 data input
GPIO131	0, 4, 8, 12				I/O	General-purpose input/output 131
SD2_C1	7	V10	–	–	I	Sigma-Delta 2 channel 1 clock input
GPIO132	0, 4, 8, 12				I/O	General-purpose input/output 132
SD2_D2	7	W18	–	–	I	Sigma-Delta 2 channel 2 data input
GPIO133/AUXCLKIN	0, 4, 8, 12				I/O	General-purpose input/output 133. The AUXCLKIN function of this GPIO pin could be used to provide a single-ended 3.3-V level clock signal to the Auxiliary Phase-Locked Loop (APLL), whose output is used for the USB module. The AUXCLKIN clock may also be used for the CAN module.
SD2_C2	7	G18	118	–	I	Sigma-Delta 2 channel 2 clock input
GPIO134	0, 4, 8, 12				I/O	General-purpose input/output 134
SD2_D3	7	V18	–	–	I	Sigma-Delta 2 channel 3 data input
GPIO135	0, 4, 8, 12				I/O	General-purpose input/output 135
SCITXDA	6	U18	–	–	O	SCI-A transmit data
SD2_C3	7				I	Sigma-Delta 2 channel 3 clock input
GPIO136	0, 4, 8, 12				I/O	General-purpose input/output 136
SCIRXDA	6	T17	–	–	I	SCI-A receive data
SD2_D4	7				I	Sigma-Delta 2 channel 4 data input

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO137 SCITXDB SD2_C4	0, 4, 8, 12 6 7	T18	–	–	I/O O I	General-purpose input/output 137 SCI-B transmit data Sigma-Delta 2 channel 4 clock input
GPIO138 SCIRXDB	0, 4, 8, 12 6	T19	–	–	I/O I	General-purpose input/output 138 SCI-B receive data
GPIO139 SCIRXDC	0, 4, 8, 12 6	N19	–	–	I/O I	General-purpose input/output 139 SCI-C receive data
GPIO140 SCITXDC	0, 4, 8, 12 6	M19	–	–	I/O O	General-purpose input/output 140 SCI-C transmit data
GPIO141 SCIRXDD	0, 4, 8, 12 6	M18	–	–	I/O I	General-purpose input/output 141 SCI-D receive data
GPIO142 SCITXDD	0, 4, 8, 12 6	L19	–	–	I/O O	General-purpose input/output 142 SCI-D transmit data
GPIO143	0, 4, 8, 12	F18	–	–	I/O	General-purpose input/output 143
GPIO144	0, 4, 8, 12	F17	–	–	I/O	General-purpose input/output 144
GPIO145 EPWM1A	0, 4, 8, 12 1	E17	–	–	I/O O	General-purpose input/output 145 Enhanced PWM1 output A and HRPWM channel
GPIO146 EPWM1B	0, 4, 8, 12 1	D18	–	–	I/O O	General-purpose input/output 146 Enhanced PWM1 output B and HRPWM channel
GPIO147 EPWM2A	0, 4, 8, 12 1	D17	–	–	I/O O	General-purpose input/output 147 Enhanced PWM2 output A and HRPWM channel
GPIO148 EPWM2B	0, 4, 8, 12 1	D14	–	–	I/O O	General-purpose input/output 148 Enhanced PWM2 output B and HRPWM channel
GPIO149 EPWM3A	0, 4, 8, 12 1	A13	–	–	I/O O	General-purpose input/output 149 Enhanced PWM3 output A and HRPWM channel
GPIO150 EPWM3B	0, 4, 8, 12 1	B13	–	–	I/O O	General-purpose input/output 150 Enhanced PWM3 output B and HRPWM channel
GPIO151 EPWM4A	0, 4, 8, 12 1	C13	–	–	I/O O	General-purpose input/output 151 Enhanced PWM4 output A and HRPWM channel
GPIO152 EPWM4B	0, 4, 8, 12 1	D13	–	–	I/O O	General-purpose input/output 152 Enhanced PWM4 output B and HRPWM channel
GPIO153 EPWM5A	0, 4, 8, 12 1	A12	–	–	I/O O	General-purpose input/output 153 Enhanced PWM5 output A and HRPWM channel
GPIO154 EPWM5B	0, 4, 8, 12 1	B12	–	–	I/O O	General-purpose input/output 154 Enhanced PWM5 output B and HRPWM channel
GPIO155 EPWM6A	0, 4, 8, 12 1	C12	–	–	I/O O	General-purpose input/output 155 Enhanced PWM6 output A and HRPWM channel
GPIO156 EPWM6B	0, 4, 8, 12 1	D12	–	–	I/O O	General-purpose input/output 156 Enhanced PWM6 output B and HRPWM channel
GPIO157 EPWM7A	0, 4, 8, 12 1	B10	–	–	I/O O	General-purpose input/output 157 Enhanced PWM7 output A and HRPWM channel
GPIO158 EPWM7B	0, 4, 8, 12 1	C10	–	–	I/O O	General-purpose input/output 158 Enhanced PWM7 output B and HRPWM channel
GPIO159 EPWM8A	0, 4, 8, 12 1	D10	–	–	I/O O	General-purpose input/output 159 Enhanced PWM8 output A and HRPWM channel

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
GPIO160 EPWM8B	0, 4, 8, 12 1	B9	–	–	I/O O	General-purpose input/output 160 Enhanced PWM8 output B and HRPWM channel
GPIO161 EPWM9A	0, 4, 8, 12 1	C9	–	–	I/O O	General-purpose input/output 161 Enhanced PWM9 output A
GPIO162 EPWM9B	0, 4, 8, 12 1	D9	–	–	I/O O	General-purpose input/output 162 Enhanced PWM9 output B
GPIO163 EPWM10A	0, 4, 8, 12 1	A8	–	–	I/O O	General-purpose input/output 163 Enhanced PWM10 output A
GPIO164 EPWM10B	0, 4, 8, 12 1	B8	–	–	I/O O	General-purpose input/output 164 Enhanced PWM10 output B
GPIO165 EPWM11A	0, 4, 8, 12 1	C5	–	–	I/O O	General-purpose input/output 165 Enhanced PWM11 output A
GPIO166 EPWM11B	0, 4, 8, 12 1	D5	–	–	I/O O	General-purpose input/output 166 Enhanced PWM11 output B
GPIO167 EPWM12A	0, 4, 8, 12 1	C4	–	–	I/O O	General-purpose input/output 167 Enhanced PWM12 output A
GPIO168 EPWM12B	0, 4, 8, 12 1	D4	–	–	I/O O	General-purpose input/output 168 Enhanced PWM12 output B

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
RESET						
$\overline{\text{XRS}}$		F19	124	69	I/OD	Device reset (in) and watchdog reset (out). This device has built-in power-on reset circuitry. During a power-on condition, this pin is driven low by the device. This pin is also driven low by the MCU when a watchdog or non-maskable interrupt (NMI) watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for 512 INTOSC1 cycles. External circuitry may also drive this pin to assert a device reset. In this case, it is recommended that this pin be driven by an open-drain device. An R-C circuit must be connected to this pin for noise immunity reasons. Regardless of the source, a device reset causes the device to terminate execution. When reset is deactivated, execution begins at the reset vector in the boot ROM. The output buffer of this pin is an open-drain with an internal pullup. This pin has an internal 300-ns (nominal) glitch filter.
CLOCKS						
X1		G19	123	68	I	On-chip crystal-oscillator input. To use this oscillator, a quartz crystal must be connected across X1 and X2. If this pin is not used, it must be tied to GND. This pin can also be used to feed a single-ended 3.3-V level clock. In this case, X2 is a No Connect (NC).
X2		J19	121	66	O	On-chip crystal-oscillator output. A quartz crystal may be connected across X1 and X2. If X2 is not used, it must be left unconnected.
NO CONNECT						
NC		H4	–	–		No connect. BGA ball is electrically open and not connected to the die.
JTAG						
TCK		V15	81	50	I	JTAG test clock with internal pullup (see Section 5.4)
TDI		W13	77	46	I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO		W15	78	47	O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (6-mA drive). ⁽⁶⁾
TMS		W14	80	49	I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
$\overline{\text{TRST}}$		V14	79	48	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: $\overline{\text{TRST}}$ is an active-low test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-k Ω resistor generally offers adequate protection. Since the value of the resistor is application-specific, TI recommends that each target board be validated for proper operation of the debugger and the application. This pin has an internal 50-ns (nominal) glitch filter.
INTERNAL VOLTAGE REGULATOR CONTROL						
VREGENZ		J18	119	64	I	Internal voltage regulator enable with internal pulldown. The internal VREG is not supported and must be disabled. Connect VREGENZ to V _{DDIO} .

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
ANALOG, DIGITAL, AND I/O POWER						
V _{DD}		E9	16	16		1.2-V digital logic power pins. Place a decoupling capacitor on each V _{DD} pin such that the total capacitance on the V _{DD} supply rail is evenly distributed and between 12 µF and 26.5 µF.
		E11	21	39		
		F9	61	45		
		F11	76	63		
		G14	117	71		
		G15	126	78		
		J14	137	84		
		J15	153	89		
		K5	158	95		
		K6	169	–		
		P10	–	–		
		P13	–	–		
		R10	–	–		
	R13	–	–			
V _{DD3VFL}		R11	72	41		3.3-V Flash power pin. Place a minimum 0.1-µF decoupling capacitor on each pin.
		R12	–	–		
V _{DDA}		P6	36	18		3.3-V analog power pins. Place a minimum 2.2-µF decoupling capacitor on each pin.
		R6	54	38		

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
V _{DDIO}		A9	3	2		3.3-V digital I/O power pins. Place a minimum 0.1-μF decoupling capacitor on each pin.
		A18	11	10		
		B1	15	15		
		E7	20	40		
		E10	26	44		
		E13	62	55		
		E16	68	62		
		F4	75	72		
		F7	82	79		
		F10	88	83		
		F13	91	90		
		F16	99	94		
		G4	106	–		
		G5	114	–		
		G6	116	–		
		H5	127	–		
		H6	138	–		
		L14	147	–		
		L15	152	–		
		M1	159	–		
		M5	168	–		
	M6	–	–			
	N14	–	–			
	N15	–	–			
	P9	–	–			
	R9	–	–			
	V19	–	–			
	W8	–	–			
V _{DDOSC}		H16	120	65		3.3-V on-chip crystal oscillator (X1 and X2) power pins. Place a minimum 0.1-μF decoupling capacitor on each pin.
		H17	125	70		

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
V _{SS}		A1	PWR PAD	PWR PAD		Analog and digital ground. For Quad Flatpacks (QFPs), the PowerPad on the bottom of the package must be soldered to the ground plane of the PCB.
		A10				
		A19				
		E5				
		E6				
		E8				
		E12				
		E14				
		E15				
		F5				
		F6				
		F8				
		F12				
		F14				
		F15				
		G16				
		G17				
		H8				
		H9				
		H10				
		H11				
		H12				
		H14				
		H15				
		J5				
		J6				
		J8				
		J9				
		J10				
		J11				
	J12					
	K8					
	K9					
	K10					
	K11					
	K12					
	K14					
	K15					
	L5					
	L6					
	L8					
	L9					

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

NAME	TERMINAL				I/O/Z ⁽¹⁾	DESCRIPTION
	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
V _{SS}		L10	PWR PAD	PWR PAD		Analog and digital ground power pad (located on the bottom of the chip for quad flatpacks).
		L11				
		L12				
		L18				
		M8				
		M9				
		M10				
		M11				
		M12				
		M14				
		M15				
		N1				
		N5				
		N6				
		P7				
		P8				
		P11				
		P12				
		P14				
	P15					
	R7					
	R8					
	R14					
	R15					
	W7					
	W19					
V _{SSOSC}		H18	122	67		Crystal oscillator (X1 and X2) ground pin. When using an external crystal, do not connect this pin to the board ground. Instead, connect it to the ground reference of the external crystal oscillator circuit. If an external crystal is not used, this pin may be connected to the board ground.
		H19	–	–		
V _{SSA}		P1	34	17		Analog module ground pins. On the PZP package, pin 17 is double-bonded to V _{SSA} and V _{REFLOA} . This pin must be connect to V _{SSA} .
		P5	52	35		
		R5	–	36		
		V7	–	–		
		W1	–	–		

ADVANCE INFORMATION

Table 4-1. Signal Descriptions (continued)

TERMINAL					I/O/Z ⁽¹⁾	DESCRIPTION
NAME	MUX POSITION	ZWT BALL NO.	PTP PIN NO.	PZP PIN NO.		
SPECIAL FUNCTIONS						
ERRORSTS		U19	92	–	O	Error status output. This pin has pulldown.
TEST PINS						
FLT1		W12	73	42	I/O	Flash test pin 1. Reserved for TI. Must be left unconnected.
FLT2		V13	74	43	I/O	Flash test pin 2. Reserved for TI. Must be left unconnected.

(1) I = Input, O = Output, OD = Open Drain, Z = High Impedance

(2) ADCINB0/VDAC has an internal 100-pF capacitor to V_{SSA} .

(3) The maximum toggling frequency of the GPIOs is 50 MHz.

(4) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

(5) This pin has output impedance that can be as low as 22Ω. This output could have fast edges and ringing depending on the system PCB characteristics. If this is a concern, the user should take precautions such as adding a 39Ω (10% tolerance) series termination resistor or implement some other termination scheme. It is also recommended that a system-level signal integrity analysis be performed with the provided IBIS models. The termination is not required if this pin is used for input function.

4.2 Pin Multiplexing

4.2.1 GPIO Muxed Pins

Table 4-2 shows the GPIO muxed pins. The default for each pin is the GPIO function, secondary functions can be selected by setting both the GPyGMUXn.GPIOz and GPyMUXn.GPIOz register bits. The GPyGMUXn register should be configured prior to the GPyMUXn to avoid transient pulses on GPIO's from alternate mux selections. Columns not shown and blank cells are reserved GPIO Mux settings.

Table 4-2. GPIO Muxed Pins⁽¹⁾⁽²⁾

GPIO Index	GPIO Mux Selection							
	0, 4, 8, 12	1	2	3	5	6	7	15
	GPyGMUXn. GPIOz = 00b, 01b, 10b, 11b	00b			01b			11b
GPyMUXn. GPIOz =	00b	01b	10b	11b	01b	10b	11b	11b
GPIO0	EPWM1A (O)					SDAA (I/OD)		
GPIO1	EPWM1B (O)			MFSRB (I/O)		SCLA (I/OD)		
GPIO2	EPWM2A (O)				OUTPUTXBAR1 (O)	SDAB (I/OD)		
GPIO3	EPWM2B (O)	OUTPUTXBAR2 (O)		MCLKRB (I/O)	OUTPUTXBAR2 (O)	SCLB (I/OD)		
GPIO4	EPWM3A (O)				OUTPUTXBAR3 (O)	CANTXA (O)		
GPIO5	EPWM3B (O)	MFSRA (I/O)		OUTPUTXBAR3 (O)		CANRXA (I)		
GPIO6	EPWM4A (O)	OUTPUTXBAR4 (O)	EPWMSYNCO (O)	EQEP3A (I)		CANTXB (O)		
GPIO7	EPWM4B (O)	MCLKRA (I/O)	OUTPUTXBAR5 (O)	EQEP3B (I)		CANRXB (I)		
GPIO8	EPWM5A (O)	CANTXB (O)	ADCSOAO (O)	EQEP3S (I/O)		SCITXDA (O)		
GPIO9	EPWM5B (O)	SCITXDB (O)	OUTPUTXBAR6 (O)	EQEP3I (I/O)		SCIRXDA (I)		
GPIO10	EPWM6A (O)	CANRXB (I)	ADCSOCHO (O)	EQEP1A (I)		SCITXDB (O)		UPP-WAIT (I/O)
GPIO11	EPWM6B (O)	SCIRXDB (I)	OUTPUTXBAR7 (O)	EQEP1B (I)		SCIRXDB (I)		UPP-STRT (I/O)
GPIO12	EPWM7A (O)	CANTXB (O)	MDXB (O)	EQEP1S (I/O)		SCITXDC (O)		UPP-ENA (I/O)
GPIO13	EPWM7B (O)	CANRXB (I)	MDRB (I)	EQEP11 (I/O)		SCIRXDC (I)		UPP-D7 (I/O)
GPIO14	EPWM8A (O)	SCITXDB (O)	MCLKXB (I/O)			OUTPUTXBAR3 (O)		UPP-D6 (I/O)
GPIO15	EPWM8B (O)	SCIRXDB (I)	MFSXB (I/O)			OUTPUTXBAR4 (O)		UPP-D5 (I/O)
GPIO16	SPISIMOA (I/O)	CANTXB (O)	OUTPUTXBAR7 (O)	EPWM9A (O)			SD1_D1 (I)	UPP-D4 (I/O)
GPIO17	SPISOMIA (I/O)	CANRXB (I)	OUTPUTXBAR8 (O)	EPWM9B (O)			SD1_C1 (I)	UPP-D3 (I/O)
GPIO18	SPICLKA (I/O)	SCITXDB (O)	CANRXA (I)	EPWM10A (O)			SD1_D2 (I)	UPP-D2 (I/O)
GPIO19	SPISTEA (I/O)	SCIRXDB (I)	CANTXA (O)	EPWM10B (O)			SD1_C2 (I)	UPP-D1 (I/O)
GPIO20	EQEP1A (I)	MDXA (O)	CANTXB (O)	EPWM11A (O)			SD1_D3 (I)	UPP-D0 (I/O)
GPIO21	EQEP1B (I)	MDRA (I)	CANRXB (I)	EPWM11B (O)			SD1_C3 (I)	UPP-CLK (I/O)
GPIO22	EQEP1S (I/O)	MCLKXA (I/O)	SCITXDB (O)	EPWM12A (O)		SPICLKB (I/O)	SD1_D4 (I)	
GPIO23	EQEP11 (I/O)	MFSXA (I/O)	SCIRXDB (I)	EPWM12B (O)		SPISTEB (I/O)	SD1_C4 (I)	
GPIO24	OUTPUTXBAR1 (O)	EQEP2A (I)	MDXB (O)			SPISIMOB (I/O)	SD2_D1 (I)	
GPIO25	OUTPUTXBAR2 (O)	EQEP2B (I)	MDRB (I)			SPISOMIB (I/O)	SD2_C1 (I)	
GPIO26	OUTPUTXBAR3 (O)	EQEP2I (I/O)	MCLKXB (I/O)	OUTPUTXBAR3 (O)		SPICLKB (I/O)	SD2_D2 (I)	
GPIO27	OUTPUTXBAR4 (O)	EQEP2S (I/O)	MFSXB (I/O)	OUTPUTXBAR4 (O)		SPISTEB (I/O)	SD2_C2 (I)	
GPIO28	SCIRXDA (I)	EM1CS4 (O)		OUTPUTXBAR5 (O)		EQEP3A (I)	SD2_D3 (I)	
GPIO29	SCITXDA (O)	EM1SDCKE (O)		OUTPUTXBAR6 (O)		EQEP3B (I)	SD2_C3 (I)	
GPIO30	CANRXA (I)	EM1CLK (O)		OUTPUTXBAR7 (O)		EQEP3S (I/O)	SD2_D4 (I)	
GPIO31	CANTXA (O)	EM1WE (O)		OUTPUTXBAR8 (O)		EQEP3I (I/O)	SD2_C4 (I)	
GPIO32	SDAA (I/OD)	EM1CS0 (O)						
GPIO33	SCLA (I/OD)	EM1RNW (O)						
GPIO34	OUTPUTXBAR1 (O)	EM1CS2 (O)				SDAB (I/OD)		
GPIO35	SCIRXDA (I)	EM1CS3 (O)				SCLB (I/OD)		
GPIO36	SCITXDA (O)	EM1WAIT (I)				CANRXA (I)		
GPIO37	OUTPUTXBAR2 (O)	EM1OE (O)				CANTXA (O)		
GPIO38		EM1A0 (O)			SCITXDC (O)	CANTXB (O)		
GPIO39		EM1A1 (O)			SCIRXDC (I)	CANRXB (I)		

(1) I = Input, O = Output, OD = Open Drain

(2) GPIO Index settings of 9, 10, 11, 13, and 14 are reserved.

Table 4-2. GPIO Muxed Pins⁽¹⁾⁽²⁾ (continued)

GPIO Index	GPIO Mux Selection							
	0, 4, 8, 12	1	2	3	5	6	7	15
GPyGMUXn. GPIOz =	00b, 01b, 10b, 11b	00b			01b			11b
GPyMUXn. GPIOz =	00b	01b	10b	11b	01b	10b	11b	11b
GPIO40			EM1A2 (O)			SDAB (I/OD)		
GPIO41			EM1A3 (O)			SCLB (I/OD)		
GPIO42						SDAA (I/OD)		SCITXDA (O)
GPIO43						SCLA (I/OD)		SCIRXDA (I)
GPIO44			EM1A4 (O)					
GPIO45			EM1A5 (O)					
GPIO46			EM1A6 (O)			SCIRXDD (I)		
GPIO47			EM1A7 (O)			SCITXDD (O)		
GPIO48	OUTPUTXBAR3 (O)		EM1A8 (O)			SCITXDA (O)	SD1_D1 (I)	
GPIO49	OUTPUTXBAR4 (O)		EM1A9 (O)			SCIRXDA (I)	SD1_C1 (I)	
GPIO50	EQEP1A (I)		EM1A10 (O)			SPISIMOC (I/O)	SD1_D2 (I)	
GPIO51	EQEP1B (I)		EM1A11 (O)			SPISOMIC (I/O)	SD1_C2 (I)	
GPIO52	EQEP1S (I/O)		EM1A12 (O)			SPICLK (I/O)	SD1_D3 (I)	
GPIO53	EQEP1I (I/O)		EM1D31 (I/O)	EM2D15 (I/O)		SPISTEC (I/O)	SD1_C3 (I)	
GPIO54	SPISIMOA (I/O)		EM1D30 (I/O)	EM2D14 (I/O)	EQEP2A (I)	SCITXDB (O)	SD1_D4 (I)	
GPIO55	SPISOMIA (I/O)		EM1D29 (I/O)	EM2D13 (I/O)	EQEP2B (I)	SCIRXDB (I)	SD1_C4 (I)	
GPIO56	SPICLKA (I/O)		EM1D28 (I/O)	EM2D12 (I/O)	EQEP2S (I/O)	SCITXDC (O)	SD2_D1 (I)	
GPIO57	SPISTEA (I/O)		EM1D27 (I/O)	EM2D11 (I/O)	EQEP2I (I/O)	SCIRXDC (I)	SD2_C1 (I)	
GPIO58	MCLKRA (I/O)		EM1D26 (I/O)	EM2D10 (I/O)	OUTPUTXBAR1 (O)	SPICLKB (I/O)	SD2_D2 (I)	SPISIMOA ⁽³⁾ (I/O)
GPIO59	MFSRA (I/O)		EM1D25 (I/O)	EM2D9 (I/O)	OUTPUTXBAR2 (O)	SPISTEB (I/O)	SD2_C2 (I)	SPISOMIA ⁽³⁾ (I/O)
GPIO60	MCLKRB (I/O)		EM1D24 (I/O)	EM2D8 (I/O)	OUTPUTXBAR3 (O)	SPISIMOB (I/O)	SD2_D3 (I)	SPICLKA ⁽³⁾ (I/O)
GPIO61	MFSRB (I/O)		EM1D23 (I/O)	EM2D7 (I/O)	OUTPUTXBAR4 (O)	SPISOMIB (I/O)	SD2_C3 (I)	SPISTEA ⁽³⁾ (I/O)
GPIO62	SCIRXDC (I)		EM1D22 (I/O)	EM2D6 (I/O)	EQEP3A (I)	CANRXA (I)	SD2_D4 (I)	
GPIO63	SCITXDC (O)		EM1D21 (I/O)	EM2D5 (I/O)	EQEP3B (I)	CANTXA (O)	SD2_C4 (I)	SPISIMOB ⁽³⁾ (I/O)
GPIO64			EM1D20 (I/O)	EM2D4 (I/O)	EQEP3S (I/O)	SCIRXDA (I)		SPISOMIB ⁽³⁾ (I/O)
GPIO65			EM1D19 (I/O)	EM2D3 (I/O)	EQEP3I (I/O)	SCITXDA (O)		SPICLKB ⁽³⁾ (I/O)
GPIO66			EM1D18 (I/O)	EM2D2 (I/O)		SDAB (I/OD)		SPISTEB ⁽³⁾ (I/O)
GPIO67			EM1D17 (I/O)	EM2D1 (I/O)				
GPIO68			EM1D16 (I/O)	EM2D0 (I/O)				
GPIO69			EM1D15 (I/O)			SCLB (I/OD)		SPISIMOC ⁽³⁾ (I/O)
GPIO70			EM1D14 (I/O)		CANRXA (I)	SCITXDB (O)		SPISOMIC ⁽³⁾ (I/O)
GPIO71			EM1D13 (I/O)		CANTXA (O)	SCIRXDB (I)		SPICLK ⁽³⁾ (I/O)
GPIO72			EM1D12 (I/O)		CANTXB (O)	SCITXDC (O)		SPISTEC ⁽³⁾ (I/O)
GPIO73			EM1D11 (I/O)	XCLKOUT (O)	CANRXB (I)	SCIRXDC (I)		
GPIO74			EM1D10 (I/O)					
GPIO75			EM1D9 (I/O)					
GPIO76			EM1D8 (I/O)			SCITXDD (O)		
GPIO77			EM1D7 (I/O)			SCIRXDD (I)		
GPIO78			EM1D6 (I/O)			EQEP2A (I)		
GPIO79			EM1D5 (I/O)			EQEP2B (I)		
GPIO80			EM1D4 (I/O)			EQEP2S (I/O)		
GPIO81			EM1D3 (I/O)			EQEP2I (I/O)		
GPIO82			EM1D2 (I/O)					
GPIO83			EM1D1 (I/O)					
GPIO84					SCITXDA (O)	MDXB (O)		MDXA (O)
GPIO85			EM1D0 (I/O)		SCIRXDA (I)	MDRB (I)		MDRA (I)
GPIO86			EM1A13 (O)	EM1CAS (O)	SCITXDB (O)	MCLKXB (I/O)		MCLKXA (I/O)
GPIO87			EM1A14 (O)	EM1RAS (O)	SCIRXDB (I)	MFSXB (I/O)		MFSXA (I/O)
GPIO88			EM1A15 (O)	EM1DQM0 (O)				
GPIO89			EM1A16 (O)	EM1DQM1 (O)		SCITXDC (O)		

(3) High-Speed SPI-enabled GPIO mux option. This pin mux option is required when using the SPI in High-Speed Mode (HS_MODE = 1 in SPICCR). This mux option is still available when not using the SPI in High-Speed Mode (HS_MODE = 0 in SPICCR).

Table 4-2. GPIO Muxed Pins⁽¹⁾⁽²⁾ (continued)

GPIO Index	GPIO Mux Selection							
	0, 4, 8, 12	1	2	3	5	6	7	15
GPyGMUXn. GPIOz =	00b, 01b, 10b, 11b	00b			01b			11b
GPyMUXn. GPIOz =	00b	01b	10b	11b	01b	10b	11b	11b
GPIO90			EM1A17 (O)	EM1DQM2 (O)		SCIRXDC (I)		
GPIO91			EM1A18 (O)	EM1DQM3 (O)		SDAA (I/OD)		
GPIO92			EM1A19 (O)	EM1BA1 (O)		SCLA (I/OD)		
GPIO93				EM1BA0 (O)		SCITXDD (O)		
GPIO94						SCIRXDD (I)		
GPIO95								
GPIO96				EM2DQM1 (O)	EQEP1A (I)			
GPIO97				EM2DQM0 (O)	EQEP1B (I)			
GPIO98				EM2A0 (O)	EQEP1S (I/O)			
GPIO99				EM2A1 (O)	EQEP1I (I/O)			
GPIO100				EM2A2 (O)	EQEP2A (I)	SPISIMOC (I/O)		
GPIO101				EM2A3 (O)	EQEP2B (I)	SPISOMIC (I/O)		
GPIO102				EM2A4 (O)	EQEP2S (I/O)	SPICLK (I/O)		
GPIO103				EM2A5 (O)	EQEP2I (I/O)	SPISTEC (I/O)		
GPIO104	SDAA (I/OD)			EM2A6 (O)	EQEP3A (I)	SCITXDD (O)		
GPIO105	SCLA (I/OD)			EM2A7 (O)	EQEP3B (I)	SCIRXDD (I)		
GPIO106				EM2A8 (O)	EQEP3S (I/O)	SCITXDC (O)		
GPIO107				EM2A9 (O)	EQEP3I (I/O)	SCIRXDC (I)		
GPIO108				EM2A10 (O)				
GPIO109				EM2A11 (O)				
GPIO110				EM2WAIT (I)				
GPIO111				EM2BA0 (O)				
GPIO112				EM2BA1 (O)				
GPIO113				EM2CAS (O)				
GPIO114				EM2RAS (O)				
GPIO115				EM2CS0 (O)				
GPIO116				EM2CS2 (O)				
GPIO117				EM2SDCKE (O)				
GPIO118				EM2CLK (O)				
GPIO119				EM2RNW (O)				
GPIO120				EM2WE (O)				USB0PFLT
GPIO121				EM2OE (O)				USB0EPEN
GPIO122						SPISIMOC (I/O)	SD1_D1 (I)	
GPIO123						SPISOMIC (I/O)	SD1_C1 (I)	
GPIO124						SPICLK (I/O)	SD1_D2 (I)	
GPIO125						SPISTEC (I/O)	SD1_C2 (I)	
GPIO126							SD1_D3 (I)	
GPIO127							SD1_C3 (I)	
GPIO128							SD1_D4 (I)	
GPIO129							SD1_C4 (I)	
GPIO130							SD2_D1 (I)	
GPIO131							SD2_C1 (I)	
GPIO132							SD2_D2 (I)	
GPIO133/ AUXCLKIN							SD2_C2 (I)	
GPIO134							SD2_D3 (I)	
GPIO135						SCITXDA (O)	SD2_C3 (I)	
GPIO136						SCIRXDA (I)	SD2_D4 (I)	
GPIO137						SCITXDB (O)	SD2_C4 (I)	
GPIO138						SCIRXDB (I)		
GPIO139						SCIRXDC (I)		
GPIO140						SCITXDC (O)		

ADVANCE INFORMATION

Table 4-2. GPIO Muxed Pins⁽¹⁾⁽²⁾ (continued)

GPIO Index	GPIO Mux Selection							
	0, 4, 8, 12	1	2	3	5	6	7	15
GPyGMUXn. GPIOz =	00b, 01b, 10b, 11b	00b			01b			11b
GPyMUXn. GPIOz =	00b	01b	10b	11b	01b	10b	11b	11b
	GPIO141					SCIRXDD (I)		
	GPIO142					SCITXDD (O)		
	GPIO143							
	GPIO144							
	GPIO145	EPWM1A (O)						
	GPIO146	EPWM1B (O)						
	GPIO147	EPWM2A (O)						
	GPIO148	EPWM2B (O)						
	GPIO149	EPWM3A (O)						
	GPIO150	EPWM3B (O)						
	GPIO151	EPWM4A (O)						
	GPIO152	EPWM4B (O)						
	GPIO153	EPWM5A (O)						
	GPIO154	EPWM5B (O)						
	GPIO155	EPWM6A (O)						
	GPIO156	EPWM6B (O)						
	GPIO157	EPWM7A (O)						
	GPIO158	EPWM7B (O)						
	GPIO159	EPWM8A (O)						
	GPIO160	EPWM8B (O)						
	GPIO161	EPWM9A (O)						
	GPIO162	EPWM9B (O)						
	GPIO163	EPWM10A (O)						
	GPIO164	EPWM10B (O)						
	GPIO165	EPWM11A (O)						
	GPIO166	EPWM11B (O)						
	GPIO167	EPWM12A (O)						
	GPIO168	EPWM12B (O)						

4.2.2 USB Pin Muxing

Table 4-3 shows assignment of the alternate USB function mapping. These can be configured with the GPBAMSEL register.

Table 4-3. Alternate USB Function

GPIO	GPBAMSEL SETTING	USB FUNCTION
GPIO42	GPBAMSEL[10] = 1	USB0DM
GPIO43	GPBAMSEL[11] = 1	USB0DP

5 Specifications

5.1 Absolute Maximum Ratings^{(1) (2)}

Supply voltage range, V_{DDIO}	with respect to V_{SS}	-0.3 V to 4.6 V
Supply voltage range, V_{DSSFL}	with respect to V_{SS}	-0.3 V to 4.6 V
Supply voltage range, V_{DDOSC}	with respect to V_{SS}	-0.3 V to 4.6 V
Supply voltage range, V_{DD}	with respect to V_{SS}	-0.3 V to 1.5 V
Analog voltage range, V_{DDA}	with respect to V_{SSA}	-0.3 V to 4.6 V
Supply ramp rate (V_{DDIO} , V_{DD} , V_{DDA} , V_{DSSFL} , V_{DDOSC})	with respect to V_{SS}	$< 10^5$ V/s
Input voltage range, V_{IN} (3.3 V)		-0.3 V to 4.6 V
Output voltage range, V_O		-0.3 V to 4.6 V
Input clamp current:		
Digital input (per pin), I_{IK} ($V_{IN} < V_{SS}$ or $V_{IN} > V_{DDIO}$)		± 20 mA
Analog input (per pin), $I_{IKANALOG}$ ($V_{IN} < V_{SSA}$ or $V_{IN} > V_{DDA}$)		± 20 mA
Total for all inputs, $I_{IKTOTAL}$ ($V_{IN} < V_{SS}/V_{SSA}$ or $V_{IN} > V_{DDIO}/V_{DDA}$)		± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDIO}$)		± 20 mA
Free-Air temperature, T_A		-40°C to 125°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to conditions with absolute maximum ratings for extended periods may affect device reliability.
- (2) All voltage values are with respect to V_{SS} , unless otherwise noted.

5.2 Handling Ratings

		MIN	MAX	UNIT		
T_{stg}	Storage temperature range ⁽¹⁾	-65	150	°C		
V_{ESD}	Electrostatic discharge (ESD) ⁽²⁾ performance	Human Body Model (HBM), per AEC Q100-002 ⁽³⁾				
			All pins	-2	2	kV
		Charged Device Model (CDM), per AEC Q100-011	Corner balls on 337-ball ZWT: A1, A19, W1, W19	-500	500	V
			Corner pins on 176-pin PTP: 1, 44, 45, 88, 89, 132, 133, 176	-750	750	V
	Corner pins on 100-pin PZP: 1, 25, 26, 50, 51, 75, 76, 100					

- (1) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *IC Package Thermal Metrics Application Report* ([SPRA953](#)).
- (2) ESD measures device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
- (3) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO} ⁽¹⁾		3.14	3.3	3.47	V
Device supply voltage, V_{DD}		1.14	1.2	1.26	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA} ⁽¹⁾		3.14	3.3	3.47	V
Analog ground, V_{SSA}			0		V
Free-Air temperature, T_A	T version	-40		105	°C
	S version	-40		125	
	Q version (Q100 qualification)	-40		125	

- (1) V_{DDIO} , V_{DSSFL} , V_{DDOSC} , and V_{DDA} should be maintained within approximately 0.3 V of each other.

5.4 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = I _{OH} MAX	V _{DDIO} * 0.8			V
		I _{OH} = 50 μA	V _{DDIO} - 0.2			
V _{OL}	Low-level output voltage	I _{OL} = I _{OL} MAX	V _{DDIO} * 0.2			V
I _{OH}	High-level output source current for all GPIO pins	V _{OH} = V _{OH(MIN)}	-4			mA
I _{OL}	Low-level output sink current for all GPIO pins	V _{OL} = V _{OL(MAX)}	4			mA
I _{OZ}	Output current, pullup or pulldown disabled	V _O = V _{DDIO} or 0 V	±2			μA
V _{IH}	High-level input voltage (3.3 V)		V _{DDIO} * 0.7	V _{DDIO} + 0.3		V
V _{IL}	Low-level input voltage (3.3 V)		V _{SS} - 0.3	V _{DDIO} * 0.3		V
I _{IH}	Input current on pins with pulldown enabled	V _{DDIO} = 3.3 V, V _{IN} = V _{DDIO}	120			μA
I _{IL}	Input current on pins with pullup enabled	V _{DDIO} = 3.3 V, V _{IN} = 0 V	-150			μA
C _I	Input capacitance		2			pF

5.5 Timing and Switching Characteristics

5.5.1 Flash Timing

Table 5-1. Minimum Required Flash Wait-States at Different Frequencies

CPUCLK (MHz)	FLASH WAIT-STATES (MINIMUM REQUIRED RWAIT)
151–200	3
101–150	2
51–100	1
≤50	0

5.5.2 ADC Electrical Data and Timing

Table 5-2. ADC Characteristics (16-Bit Mode)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input clock		5		50	MHz
Sample window duration		320			ns
ADC conversion cycles			29.5		ADCCLKs
Conversion range		V_{REFLO}		V_{REFHI}	V
V_{REFHI}		1.98	2.5	V_{DDA}	V
V_{REFLO}			0		V
Gain error			± 64		LSB
Offset error ⁽¹⁾	$T_J = 30^\circ\text{C}$		± 1		mV
Offset error drift ⁽¹⁾			± 0.01		mV/°C
DNL			± 0.5		LSB
INL			± 1.5		LSB
Channel-to-channel offset error			± 2		LSB
Common mode voltage ⁽²⁾		$V_{REFCM} - 50$		$V_{REFCM} + 50$	mV

 (1) Relative to 2.5-V $V_{REFHI}-V_{REFLO}$ range.

 (2) $V_{REFCM} = (V_{REFHI} + V_{REFLO})/2$
Table 5-3. ADC Characteristics (12-Bit Mode)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input clock		1		50	MHz
Sample window duration		75			ns
ADC conversion cycles			10.5		ADCCLKs
Conversion range		V_{REFLO}		V_{REFHI}	V
V_{REFHI}		1.98	3.3	V_{DDA}	V
V_{REFLO}			0		V
Gain error			± 4		LSB
Offset error			± 4		LSB
DNL			± 0.5		LSB
INL			± 1.5		LSB
Channel-to-channel offset error			± 2		LSB
Common mode voltage ⁽¹⁾		$V_{REFCM} - 50$		$V_{REFCM} + 50$	mV

 (1) $V_{REFCM} = (V_{REFHI} + V_{REFLO})/2$

5.5.3 Temperature Sensor Electrical Data and Timing

Table 5-4. Temperature Sensor Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature accuracy			± 15		°C
Startup time			500		μs
ADC acquisition time		450			ns

5.5.4 Buffered DAC Electrical Data and Timing

Table 5-5. Buffered DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply rejection	1 Hz		70		dB
Noise			500		μV
Untrimmed offset	Midpoint corrected		±40		mV
Gain error			±2.5		% of FSR
DNL			±0.4		LSB
INL	Midpoint corrected		±2		LSB
Voltage output settling time			2		μs
Resolution			12		Bit
Output range			0.6 to ($V_{DDA} - 0.6$)		V
Maximum capacitive load			100		pF
Minimum resistive load			5		kΩ
R _{PD}			50		kΩ

5.5.5 CMPSS Electrical Data and Timing

Table 5-6. Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Comparator input referred offset			±20		mV
Comparator typical hysteresis ⁽¹⁾			7		mV

(1) Hysteresis is software-programmable to be a multiple of the typical hysteresis value. Supported multiples are 0x, 1x, 2x, 3x, and 4x.

Table 5-7. Comparator/DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC offset			1		mV
DAC gain error			-1%		
DAC static INL			±16		LSB
DAC resolution			12		Bit

5.6 Power Management

5.6.1 Power Supplies

An external power supply must be used to supply 3.3 V to V_{DDIO} and 1.2 V to V_{DD} . The internal VREG is not supported; therefore, the VREGENZ pin must be tied high to 3.3 V.

5.6.2 Power Sequencing

The voltage on V_{DDIO} should be greater than or equal to the voltage on V_{DD} at all times. V_{DDIO} and V_{DDA} should be powered up together. V_{DDA} must not exceed $V_{DDIO} + 0.3$ V. Before powering the device, no voltage larger than 0.3 V above V_{DDIO} should be applied to any digital pin, and no voltage larger than 0.3 V above V_{DDA} should be applied to any analog pin.

5.6.3 Power Monitoring

An internal power-on-reset (POR) circuit holds the device in reset and keeps the I/Os in a high-impedance state during power up. External supply voltage supervisors (SVS) can be used to monitor the voltage on the V_{DDIO} and V_{DD} rails and drive XRS low should supplies fall outside operational specifications.

5.7 Clocking

5.7.1 Clock Sources

Table 5-8 lists four possible clock sources.

Table 5-8. Possible Reference Clock Sources

CLOCK SOURCE	MODULES CLOCKED	COMMENTS
INTOSC1 ⁽¹⁾	Can be used to provide clock for: <ul style="list-style-type: none"> • Watchdog block • Main phase-locked loop (PLL) • CPU-Timer 2 	Internal oscillator 1. Zero-pin overhead 10-MHz internal oscillator.
INTOSC2 ⁽¹⁾⁽²⁾	Can be used to provide clock for: <ul style="list-style-type: none"> • Main PLL • Auxiliary PLL • CPU-Timer 2 	Internal oscillator 2. Zero-pin overhead 10-MHz internal oscillator.
XTAL ⁽¹⁾	Can be used to provide clock for: <ul style="list-style-type: none"> • Main PLL • Auxiliary PLL • CPU-Timer 2 	External crystal connected between X1 and X2 pins. On-chip crystal oscillator enables the use of external crystal/resonator to provide time base when connected to the device.
GPIO_AUXCLKIN	Can be used to provide clock for: <ul style="list-style-type: none"> • Auxiliary PLL • CPU-Timer 2 	Single-ended 3.3-V level clock source. GPIO133/AUXCLKIN pin should be used to provide the input clock.

(1) For power savings, both zero pin internal oscillators and the XTAL oscillator can be individually powered down if they are not being used by the application.

(2) On reset, internal oscillator 2 (INTOSC2) is the default clock source for both system PLL (OSCCLK) and auxiliary PLL (AUXOSCCLK).

Figure 5-1 shows the clocking options for system PLL.

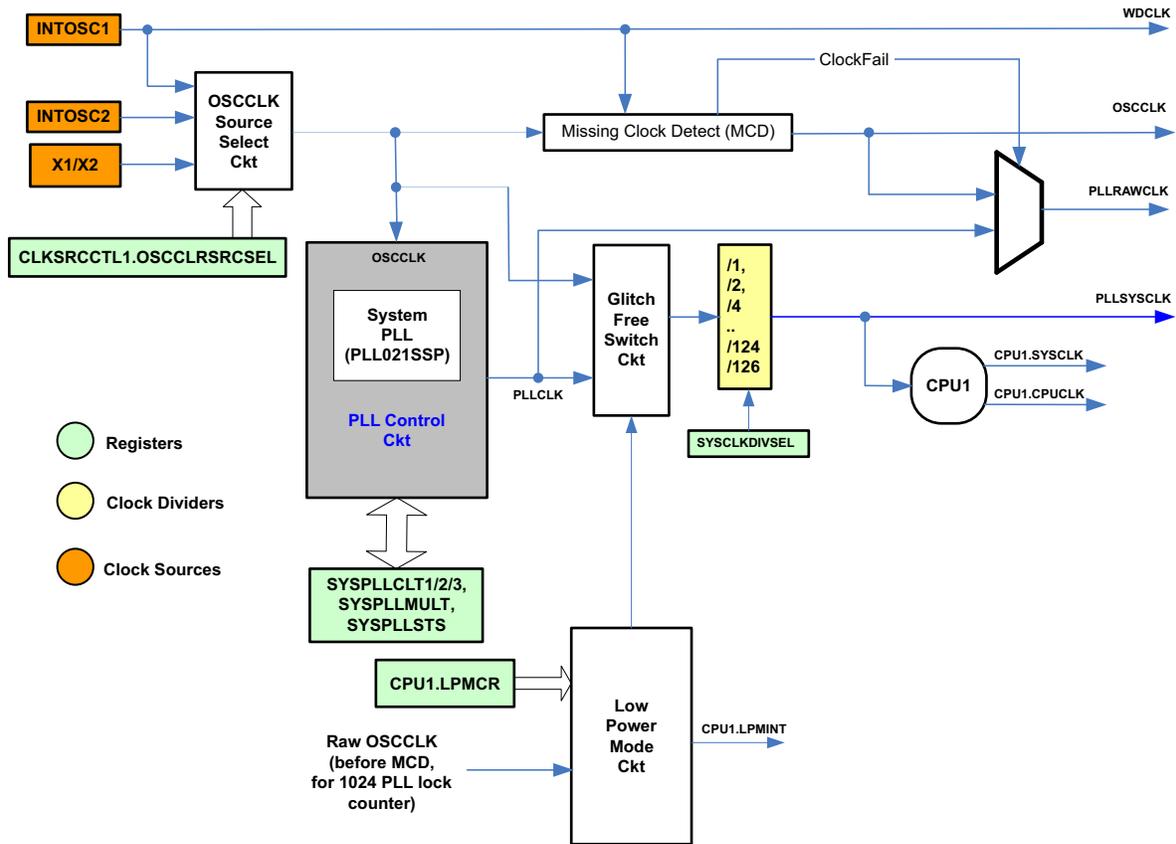


Figure 5-1. Clocking Options for System PLL

NOTE

The clock name for peripheral clocking "PERx.SYSCLK" is used interchangeably with "SYSCLKOUT" in the device documentation.

Figure 5-2 shows the clocking options for auxiliary PLL.

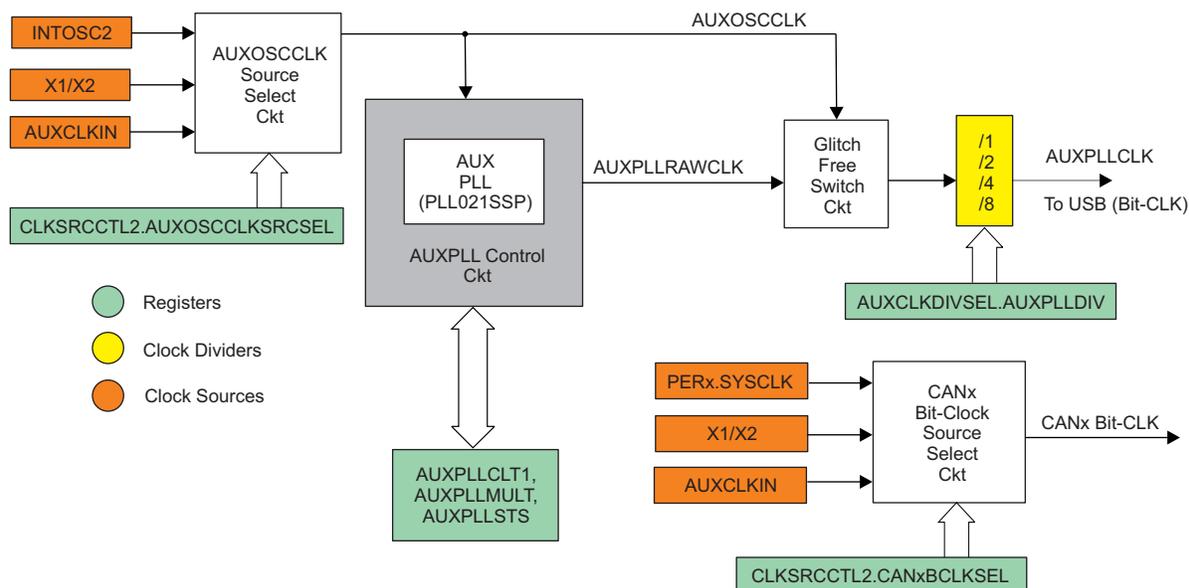


Figure 5-2. Clocking Options for Auxiliary PLL

Figure 5-3 shows the peripheral clock options.

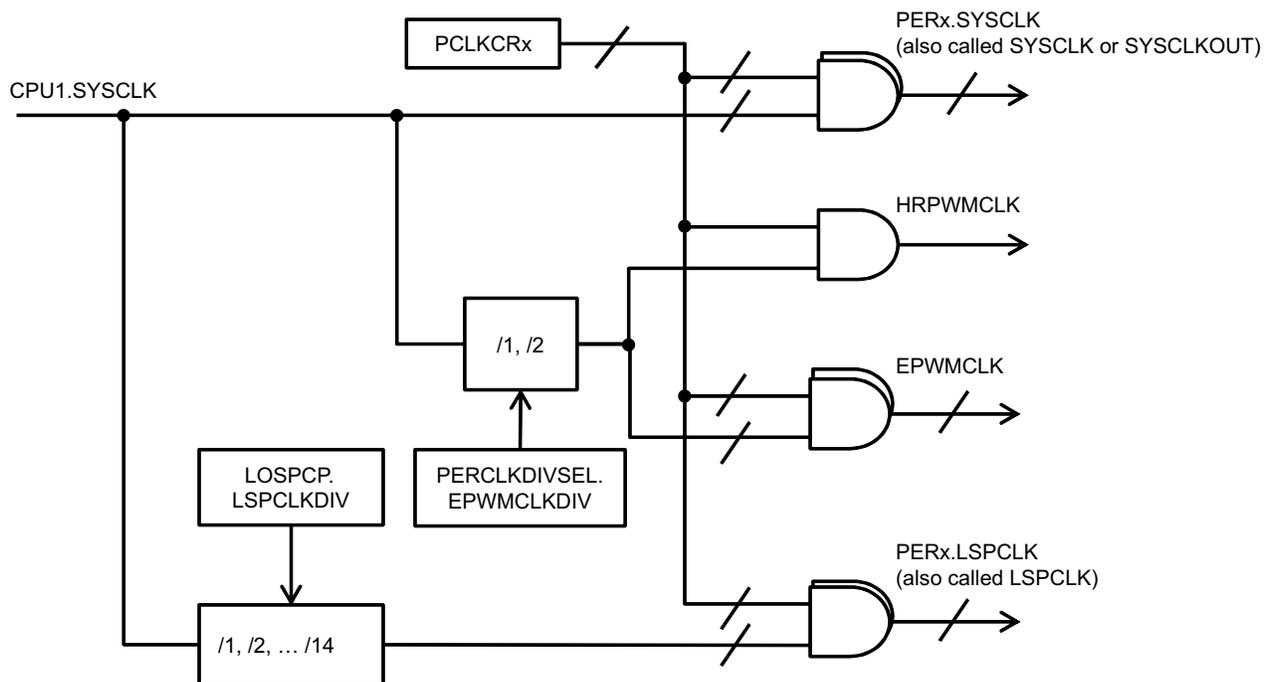


Figure 5-3. Peripheral Clock Options

ADVANCE INFORMATION

5.7.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

5.7.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

Table 5-9 shows the frequency requirements for the input clocks. Table 5-10 shows the crystal equivalent series resistance requirements. Table 5-11 and Table 5-12 show the timing requirements for the input clocks. Table 5-13 shows the PLL lock times for the Main PLL and the USB PLL.

Table 5-9. Input Clock Frequency

		MIN	MAX	UNIT
$f_{(OSC)}$	Frequency, X1/X2, from external crystal or resonator	2	20	MHz
$f_{(OCI)}$	Frequency, X1, from external oscillator (PLL enabled)	2	20	MHz
$f_{(OCI)}$	Frequency, X1, from external oscillator (PLL disabled)	2	100	MHz
$f_{(XCI)}$	Frequency, AUXCLKIN, from external oscillator	2	60	MHz

Table 5-10. Crystal Equivalent Series Resistance (ESR) Requirements⁽¹⁾

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1/2 = 12 pF)	MAXIMUM ESR (Ω) (CL1/2 = 24 pF)
2	175	375
4	100	195
6	75	145
8	65	120
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

(1) Crystal shunt capacitance (C0) should be less than or equal to 7 pF.

Table 5-11. X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(OCI)}$	Fall time, X1		6	ns
$t_{r(OCI)}$	Rise time, X1		6	ns
$t_{w(OCL)}$	Pulse duration, X1 low as a percentage of $t_{c(OCI)}$	45%	55%	
$t_{w(OCH)}$	Pulse duration, X1 high as a percentage of $t_{c(OCI)}$	45%	55%	

Table 5-12. AUXCLKIN Timing Requirements

		MIN	MAX	UNIT
$t_{f(XCI)}$	Fall time, AUXCLKIN		6	ns
$t_{r(XCI)}$	Rise time, AUXCLKIN		6	ns
$t_{w(XCL)}$	Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$	45%	55%	
$t_{w(XCH)}$	Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$	45%	55%	

Table 5-13. PLL Lock Times

		MIN	NOM	MAX	UNIT
$t_{(PLL)}$	Lock time, Main PLL (X1, from external oscillator)		2000 ⁽¹⁾		input clock cycles
$t_{(USB)}$	Lock time, USB PLL (AUXCLKIN, from external oscillator)		2000 ⁽¹⁾		input clock cycles

(1) For example, if the input clock to the PLL is 10 MHz, then the PLL lock time is 100 ns x 2000 = 200 μ s.

5.7.2.2 Internal Clock Frequencies

Table 5-14 provides the clock frequencies for the internal clocks.

Table 5-14. Internal Clock Frequencies

		MIN	NOM	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		200	MHz
$f_{(AUX)}$	Frequency, AUXPLLCLK		60		MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		200	MHz
$f_{(LSP)}$	Frequency, LSPCLK ⁽¹⁾	2	50 ⁽²⁾	200	MHz
$f_{(INT)}$	Frequency, INTOSC1/2CLK		10		MHz
$f_{(EPWM)}$	Frequency, EPWMCLK ⁽³⁾			100	MHz

(1) Lower LSPCLK will reduce device power consumption.

(2) The default at reset is SYSCLK/4.

(3) For SYSCLK above 100 MHz, the EPWMCLK must be half of SYSCLK.

5.7.2.3 Output Clock Frequency and Switching Characteristics

Table 5-15 provides the frequency of the output clock. Table 5-16 shows the switching characteristics of the output clock, XCLKOUT.

Table 5-15. Output Clock Frequency

		MIN	MAX	UNIT
$f_{(XCO)}$	Frequency, XCLKOUT	2	50	MHz

Table 5-16. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)⁽¹⁾⁽²⁾

over recommended operating conditions (unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2	H + 2	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2	H + 2	ns

(1) A load of 40 pF is assumed for these parameters.

(2) $H = 0.5t_{c(XCO)}$

5.7.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, multiple external clock source options are available. Figure 5-4 shows the recommended methods of connecting crystals, resonators, and oscillators to pins X1/X2 and AUXCLKIN.

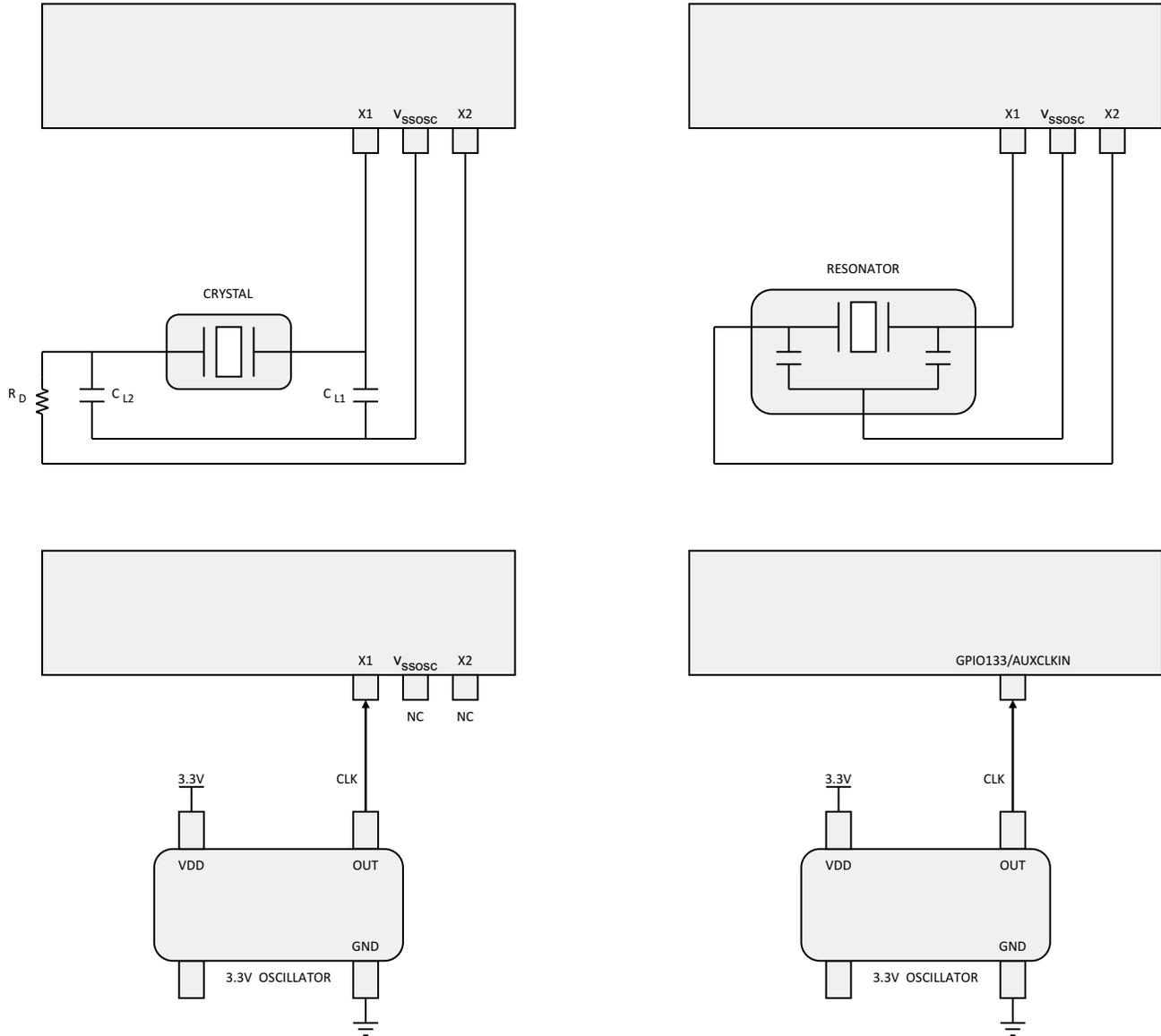


Figure 5-4. Connecting Input Clocks

ADVANCE INFORMATION

5.7.4 Oscillators

Table 5-17 provides the electrical characteristics of the two internal oscillators.

NOTE

This oscillator cannot be used as the PLL source if the PLLSYSCLK is configured to frequencies above 194 MHz.

Table 5-17. Internal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Nominal frequency			10		MHz
Frequency accuracy at room temperature	30°C		±0.1%		
Frequency accuracy across temperature	T: -40°C to 105°C S: -40°C to 125°C Q: -40°C to 125°C		±3%		
Startup and settling time			22		µs

6 Detailed Description

6.1 Functional Block Diagram

[Figure 6-1](#) shows the CPU system and associated peripherals.

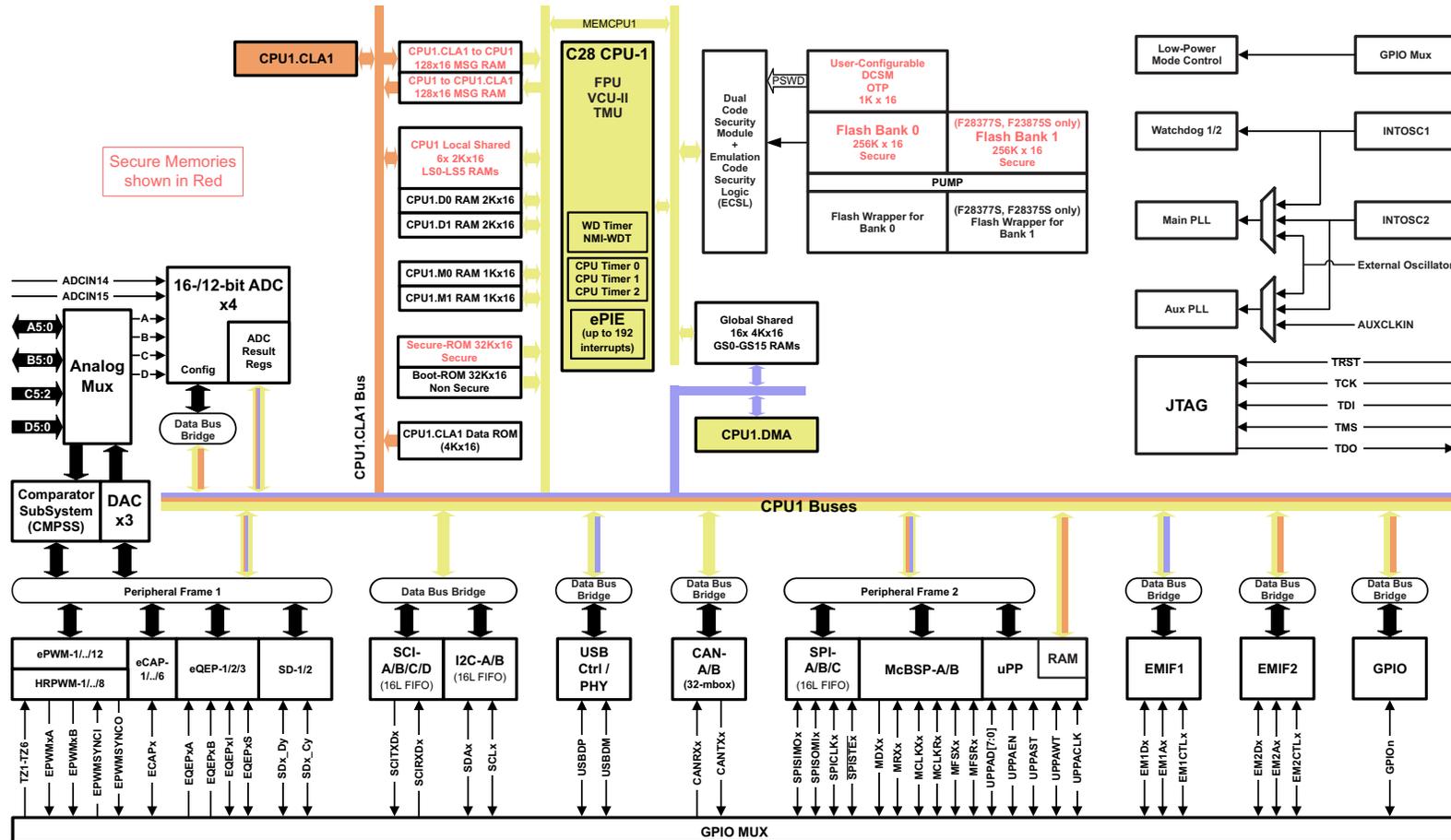


Figure 6-1. Functional Block Diagram

ADVANCE INFORMATION

6.2 Memory Maps

6.2.1 Memory Map

The C28x memory map is described in [Table 6-1](#). Memories accessible by the CLA or DMA (direct memory access) are noted as well.

Table 6-1. Memory Map

RAM	SIZE	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
M0_RAM	1K x 16	0x0000 0000	0x0000 03FF		
M1_RAM	1K x 16	0x0000 0400	0x0000 07FF		
PieVectTable	512 x 16	0x0000 0D00	0x0000 0EFF		
CPU1.CLA1_to_CPU1_MSG_RAM	128 x 16	0x0000 1480	0x0000 14FF	Yes	
CPU1_to_CPU1.CLA1_MSG_RAM	128 x 16	0x0000 1500	0x0000 157F	Yes	
UPP_TX_MSG_RAM	512 x 16	0x0000 6C00	0x0000 6DFF	Yes	
UPP_RX_MSG_RAM	512 x 16	0x0000 6E00	0x0000 6FFF	Yes	
LS0_RAM	2K x 16	0x0000 8000	0x0000 87FF	Yes	
LS1_RAM	2K x 16	0x0000 8800	0x0000 8FFF	Yes	
LS2_RAM	2K x 16	0x0000 9000	0x0000 97FF	Yes	
LS3_RAM	2K x 16	0x0000 9800	0x0000 9FFF	Yes	
LS4_RAM	2K x 16	0x0000 A000	0x0000 A7FF	Yes	
LS5_RAM	2K x 16	0x0000 A800	0x0000 AFFF	Yes	
D0_RAM	2K x 16	0x0000 B000	0x0000 B7FF		
D1_RAM	2K x 16	0x0000 B800	0x0000 BFFF		
GS0_RAM	4K x 16	0x0000 C000	0x0000 CFFF		Yes
GS1_RAM	4K x 16	0x0000 D000	0x0000 DFFF		Yes
GS2_RAM	4K x 16	0x0000 E000	0x0000 EFFF		Yes
GS3_RAM	4K x 16	0x0000 F000	0x0000 FFFF		Yes
GS4_RAM	4K x 16	0x0001 0000	0x0001 0FFF		Yes
GS5_RAM	4K x 16	0x0001 1000	0x0001 1FFF		Yes
GS6_RAM	4K x 16	0x0001 2000	0x0001 2FFF		Yes
GS7_RAM	4K x 16	0x0001 3000	0x0001 3FFF		Yes
GS8_RAM	4K x 16	0x0001 4000	0x0001 4FFF		Yes
GS9_RAM	4K x 16	0x0001 5000	0x0001 5FFF		Yes
GS10_RAM	4K x 16	0x0001 6000	0x0001 6FFF		Yes
GS11_RAM	4K x 16	0x0001 7000	0x0001 7FFF		Yes
GS12_RAM ⁽¹⁾	4K x 16	0x0001 8000	0x0001 8FFF		Yes
GS13_RAM ⁽¹⁾	4K x 16	0x0001 9000	0x0001 9FFF		Yes
GS14_RAM ⁽¹⁾	4K x 16	0x0001 A000	0x0001 AFFF		Yes
GS15_RAM ⁽¹⁾	4K x 16	0x0001 B000	0x0001 BFFF		Yes
USB_RAM	2K x 16	0x0004 1000	0x0004 17FF		Yes
CAN_A_Message_RAM	2K x 16	0x0004 8800	0x0004 97FF		
CAN_B_Message_RAM	2K x 16	0x0004 A800	0x0004 B7FF		
Flash Bank 0	256K x 16	0x0008 0000	0x000B FFFF		
Flash Bank 1	256K x 16	0x000C 0000	0x000F FFFF		
Secure_ROM	32K x 16	0x003F 0000	0x003F 7FFF		
Boot_ROM	32K x 16	0x003F 8000	0x003F FFBD		
Vectors	64	0x003F FFBE	0x003F FFFF		

(1) Only available on F28377S and F28375S.

6.2.2 Flash Memory Map

The F28377S and F28375S devices have two flash banks (256KW each) for a total of 512KW. Only one bank can be programmed or erased at a time and the code to program the flash should be executed out of RAM. The wait-states on Bank 1 reads are always one cycle greater than reads from Bank 0. See [Section 5.5.1](#) for details on flash wait-states. [Table 6-2](#) shows the addresses of flash sectors.

Table 6-2. Addresses of Flash Sectors on F28377S and F28375S

SECTOR	SIZE	START ADDRESS	END ADDRESS
OTP Sectors			
TI OTP Bank 0	1K x 16	0x0007 0000	0x0007 03FF
User configurable DCSM OTP Bank 0	1K x 16	0x0007 8000	0x0007 83FF
TI OTP Bank 1	1K x 16	0x0007 0800	0x0007 0BFF
User configurable DCSM OTP Bank 1	1K x 16	0x0007 8800	0x0007 8BFF
Bank 0 Sectors			
Sector A	8K x 16	0x0008 0000	0x0008 1FFF
Sector B	8K x 16	0x0008 2000	0x0008 3FFF
Sector C	8K x 16	0x0008 4000	0x0008 5FFF
Sector D	8K x 16	0x0008 6000	0x0008 7FFF
Sector E	32K x 16	0x0008 8000	0x0008 FFFF
Sector F	32K x 16	0x0009 0000	0x0009 7FFF
Sector G	32K x 16	0x0009 8000	0x0009 FFFF
Sector H	32K x 16	0x000A 0000	0x000A 7FFF
Sector I	32K x 16	0x000A 8000	0x000A FFFF
Sector J	32K x 16	0x000B 0000	0x000B 7FFF
Sector K	8K x 16	0x000B 8000	0x000B 9FFF
Sector L	8K x 16	0x000B A000	0x000B BFFF
Sector M	8K x 16	0x000B C000	0x000B DFFF
Sector N	8K x 16	0x000B E000	0x000B FFFF
Bank 1 Sectors			
Sector O	8K x 16	0x000C 0000	0x000C 1FFF
Sector P	8K x 16	0x000C 2000	0x000C 3FFF
Sector Q	8K x 16	0x000C 4000	0x000C 5FFF
Sector R	8K x 16	0x000C 6000	0x000C 7FFF
Sector S	32K x 16	0x000C 8000	0x000C FFFF
Sector T	32K x 16	0x000D 0000	0x000D 7FFF
Sector U	32K x 16	0x000D 8000	0x000D FFFF
Sector V	32K x 16	0x000E 0000	0x000E 7FFF
Sector W	32K x 16	0x000E 8000	0x000E FFFF
Sector X	32K x 16	0x000F 0000	0x000F 7FFF
Sector Y	8K x 16	0x000F 8000	0x000F 9FFF
Sector Z	8K x 16	0x000F A000	0x000F BFFF
Sector AA	8K x 16	0x000F C000	0x000F DFFF
Sector AB	8K x 16	0x000F E000	0x000F FFFF
Flash ECC Locations			
TI OTP ECC Bank 0	128 x 16	0x0107 0000	0x0107 007F
TI OTP ECC Bank 1	128 x 16	0x0107 0200	0x0107 027F
User OTP ECC Bank 0	128 x 16	0x0107 1000	0x0107 107F

Table 6-2. Addresses of Flash Sectors on F28377S and F28375S (continued)

SECTOR	SIZE	START ADDRESS	END ADDRESS
User OTP ECC Bank 1	128 x 16	0x0107 1200	0x0107 127F
Flash ECC Bank 0	32K x16	0x0108 0000	0x0108 7FFF
Flash ECC Bank 1	32K x16	0x0108 8000	0x0108 FFFF

The F28376S and F28374S devices have one flash bank of 256KW. See [Section 5.5.1](#) for details on flash wait-states. [Table 6-3](#) shows the addresses of flash sectors.

Table 6-3. Addresses of Flash Sectors on F28376S and F28374S

SECTOR	SIZE	START ADDRESS	END ADDRESS
OTP Sectors			
TI OTP Bank 0	1K x 16	0x0007 0000	0x0007 03FF
User configurable DCSM OTP Bank 0	1K x 16	0x0007 8000	0x0007 83FF
Bank 0 Sectors			
Sector A	8K x 16	0x0008 0000	0x0008 1FFF
Sector B	8K x 16	0x0008 2000	0x0008 3FFF
Sector C	8K x 16	0x0008 4000	0x0008 5FFF
Sector D	8K x 16	0x0008 6000	0x0008 7FFF
Sector E	32K x 16	0x0008 8000	0x0008 FFFF
Sector F	32K x 16	0x0009 0000	0x0009 7FFF
Sector G	32K x 16	0x0009 8000	0x0009 FFFF
Sector H	32K x 16	0x000A 0000	0x000A 7FFF
Sector I	32K x 16	0x000A 8000	0x000A FFFF
Sector J	32K x 16	0x000B 0000	0x000B 7FFF
Sector K	8K x 16	0x000B 8000	0x000B 9FFF
Sector L	8K x 16	0x000B A000	0x000B BFFF
Sector M	8K x 16	0x000B C000	0x000B DFFF
Sector N	8K x 16	0x000B E000	0x000B FFFF
Flash ECC Locations			
TI OTP ECC Bank 0	128 x 16	0x0107 0000	0x0107 007F
User OTP ECC Bank 0	128 x 16	0x0107 1000	0x0107 107F
Flash ECC Bank 0	32K x16	0x0108 0000	0x0108 7FFF

6.2.3 EMIF Chip Select Memory Map

The EMIF memory map is shown in [Table 6-4](#).

Table 6-4. EMIF Chip Select Memory Map

EMIF CHIP SELECT	SIZE	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
EMIF1_CS0n - Data	256M x 16	0x8000 0000	0x8FFF FFFF		Yes
EMIF1_CS2n - Program + Data	2M x 16	0x0010 0000	0x002F FFFF		Yes
EMIF1_CS3n - Program + Data	512K x 16	0x0030 0000	0x0037 FFFF		Yes
EMIF1_CS4n - Program + Data	393K x 16	0x0038 0000	0x003D FFFF		Yes
EMIF2_CS0n - Data	256M x 16	0x9000 0000	0x9FFF FFFF		
EMIF2_CS2n - Program + Data	4K x 16	0x0000 2000	0x0000 2FFF	Yes (Data only)	

6.2.4 Peripheral Registers Memory Map

The peripheral registers memory map can be found in [Table 6-5](#). Registers in the peripheral frames share a secondary master (CLA or DMA) selection with all other registers within the same peripheral frame. See the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual* ([SPRUHX5](#)) for details on the CPU subsystem and secondary master selection.

Table 6-5. Peripheral Registers Memory Map

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
AdcaResultRegs	ADC_RESULT_REGS	0x0000 0B00	0x0000 0B1F	Yes	Yes
AdcbResultRegs	ADC_RESULT_REGS	0x0000 0B20	0x0000 0B3F	Yes	Yes
AdccResultRegs	ADC_RESULT_REGS	0x0000 0B40	0x0000 0B5F	Yes	Yes
AdcdResultRegs	ADC_RESULT_REGS	0x0000 0B60	0x0000 0B7F	Yes	Yes
CpuTimer0Regs	CPU_TIMER_REGS	0x0000 0C00	0x0000 3C07		
CpuTimer1Regs	CPU_TIMER_REGS	0x0000 0C08	0x0000 5C0F		
CpuTimer2Regs	CPU_TIMER_REGS	0x0000 0C10	0x0000 C17F		
PieCtrlRegs	PIE_CTRL_REGS	0x0000 0CE0	0x0000 0CFF		
DmaRegs	DMA_REGS	0x0000 1000	0x0000 11FF		
Cla1Regs	CLA_REGS	0x0000 1400	0x0000 147F		
Peripheral Frame 1					
EPwm1Regs	EPWM_REGS	0x0000 4000	0x0000 40FF	Yes	Yes
EPwm2Regs	EPWM_REGS	0x0000 4100	0x0000 41FF	Yes	Yes
EPwm3Regs	EPWM_REGS	0x0000 4200	0x0000 42FF	Yes	Yes
EPwm4Regs	EPWM_REGS	0x0000 4300	0x0000 43FF	Yes	Yes
EPwm5Regs	EPWM_REGS	0x0000 4400	0x0000 44FF	Yes	Yes
EPwm6Regs	EPWM_REGS	0x0000 4500	0x0000 45FF	Yes	Yes
EPwm7Regs	EPWM_REGS	0x0000 4600	0x0000 46FF	Yes	Yes
EPwm8Regs	EPWM_REGS	0x0000 4700	0x0000 47FF	Yes	Yes
EPwm9Regs	EPWM_REGS	0x0000 4800	0x0000 48FF	Yes	Yes
EPwm10Regs	EPWM_REGS	0x0000 4900	0x0000 49FF	Yes	Yes
EPwm11Regs	EPWM_REGS	0x0000 4A00	0x0000 4AFF	Yes	Yes
EPwm12Regs	EPWM_REGS	0x0000 4B00	0x0000 4BFF	Yes	Yes
ECap1Regs	ECAP_REGS	0x0000 5000	0x0000 501F	Yes	Yes
ECap2Regs	ECAP_REGS	0x0000 5020	0x0000 503F	Yes	Yes
ECap3Regs	ECAP_REGS	0x0000 5040	0x0000 505F	Yes	Yes
ECap4Regs	ECAP_REGS	0x0000 5060	0x0000 507F	Yes	Yes
ECap5Regs	ECAP_REGS	0x0000 5080	0x0000 509F	Yes	Yes

Table 6-5. Peripheral Registers Memory Map (continued)

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
ECap6Regs	ECAP_REGS	0x0000 50A0	0x0000 50BF	Yes	Yes
EQep1Regs	EQEP_REGS	0x0000 5100	0x0000 513F	Yes	Yes
EQep2Regs	EQEP_REGS	0x0000 5140	0x0000 517F	Yes	Yes
EQep3Regs	EQEP_REGS	0x0000 5180	0x0000 51BF	Yes	Yes
DacaRegs	DAC_REGS	0x0000 5C00	0x0000 5C0F	Yes	Yes
DacbRegs	DAC_REGS	0x0000 5C10	0x0000 5C1F	Yes	Yes
DaccRegs	DAC_REGS	0x0000 5C20	0x0000 5C2F	Yes	Yes
Cmpss1Regs	CMPSS_REGS	0x0000 5C80	0x0000 5C9F	Yes	Yes
Cmpss2Regs	CMPSS_REGS	0x0000 5CA0	0x0000 5CBF	Yes	Yes
Cmpss3Regs	CMPSS_REGS	0x0000 5CC0	0x0000 5CDF	Yes	Yes
Cmpss4Regs	CMPSS_REGS	0x0000 5CE0	0x0000 5CFF	Yes	Yes
Cmpss5Regs	CMPSS_REGS	0x0000 5D00	0x0000 5D1F	Yes	Yes
Cmpss6Regs	CMPSS_REGS	0x0000 5D20	0x0000 5D3F	Yes	Yes
Cmpss7Regs	CMPSS_REGS	0x0000 5D40	0x0000 5D5F	Yes	Yes
Cmpss8Regs	CMPSS_REGS	0x0000 5D60	0x0000 5D7F	Yes	Yes
Sdfm1Regs	SDFM_REGS	0x0000 5E00	0x0000 5E7F	Yes	Yes
Sdfm2Regs	SDFM_REGS	0x0000 5E80	0x0000 5EFF	Yes	Yes
Peripheral Frame 2					
McbspaRegs	MCBSP_REGS	0x0000 6000	0x0000 603F	Yes	Yes
McbspbRegs	MCBSP_REGS	0x0000 6040	0x0000 607F	Yes	Yes
SpiaRegs	SPI_REGS	0x0000 6100	0x0000 610F	Yes	Yes
SpibRegs	SPI_REGS	0x0000 6110	0x0000 611F	Yes	Yes
SpicRegs	SPI_REGS	0x0000 6120	0x0000 612F	Yes	Yes
UppRegs	UPP_REGS	0x0000 6200	0x0000 62FF	Yes	Yes
Peripheral Frame 3					
WdRegs	WD_REGS	0x0000 7000	0x0000 703F		
NmiIntruptRegs	NMI_INTRUPT_REGS	0x0000 7060	0x0000 706F		
XintRegs	XINT_REGS	0x0000 7070	0x0000 707F		
SciaRegs	SCI_REGS	0x0000 7200	0x0000 720F		
ScibRegs	SCI_REGS	0x0000 7210	0x0000 721F		
ScicRegs	SCI_REGS	0x0000 7220	0x0000 722F		
ScidRegs	SCI_REGS	0x0000 7230	0x0000 723F		
I2caRegs	I2C_REGS	0x0000 7300	0x0000 733F		
I2cbRegs	I2C_REGS	0x0000 7340	0x0000 737F		
AdcaRegs	ADC_REGS	0x0000 7400	0x0000 747F	Yes	
AdcbRegs	ADC_REGS	0x0000 7480	0x0000 74FF	Yes	
AdccRegs	ADC_REGS	0x0000 7500	0x0000 757F	Yes	
AdcdRegs	ADC_REGS	0x0000 7580	0x0000 75FF	Yes	
InputXbarRegs	INPUT_XBAR_REGS	0x0000 7900	0x0000 793F		
TrigRegs	TRIG_REGS	0x0000 7940	0x0000 794F		
DmaClaSrcSelRegs	DMA_CLA_SRC_SEL_REGS	0x0000 7980	0x0000 798F		
EPwmXbarRegs	EPWM_XBAR_REGS	0x0000 7A00	0x0000 7A3F		
OutputXbarRegs	OUTPUT_XBAR_REGS	0x0000 7A80	0x0000 7ABF		
GpioCtrlRegs	GPIO_CTRL_REGS	0x0000 7C00	0x0000 7D7F		
GpioDataRegs	GPIO_DATA_REGS	0x0000 7F00	0x0000 7F2F	Yes	
UsbaRegs	USB_REGS	0x0004 0000	0x0004 0FFF		
Emif1Regs	EMIF_REGS	0x0004 7000	0x0004 77FF		

Table 6-5. Peripheral Registers Memory Map (continued)

REGISTERS	STRUCTURE NAME	START ADDRESS	END ADDRESS	CLA ACCESS	DMA ACCESS
Emif2Regs	EMIF_REGS	0x0004 7800	0x0004 7FFF		
CanaRegs	CAN_REGS	0x0004 8000	0x0004 87FF		
CanbRegs	CAN_REGS	0x0004 A000	0x0004 A7FF		
DevCfgRegs	DEV_CFG_REGS	0x0005 D000	0x0005 D17F		
AnalogSubsysRegs	ANALOG_SUBSYS_REGS	0x0005 D180	0x0005 D1FF		
ClkCfgRegs	CLK_CFG_REGS	0x0005 D200	0x0005 D2FF		
CpuSysRegs	CPU_SYS_REGS	0x0005 D300	0x0005 D3FF		
RomPrefetchRegs	ROM_PREFETCH_REGS	0x0005 E608	0x0005 E60B		
DcsmZ1Regs	DCSM_Z1_REGS	0x0005 F000	0x0005 F02F		
DcsmZ2Regs	DCSM_Z2_REGS	0x0005 F040	0x0005 F05F		
DcsmCommonRegs	DCSM_COMMON_REGS	0x0005 F070	0x0005 F07F		
MemCfgRegs	MEM_CFG_REGS	0x0005 F400	0x0005 F47F		
Emif1ConfigRegs	EMIF1_CONFIG_REGS	0x0005 F480	0x0005 F49F		
Emif2ConfigRegs	EMIF2_CONFIG_REGS	0x0005 F4A0	0x0005 F4BF		
AccessProtectionRegs	ACCESS_PROTECTION_REGS	0x0005 F4C0	0x0005 F4FF		
MemoryErrorRegs	MEMORY_ERROR_REGS	0x0005 F500	0x0005 F53F		
RomWaitStateRegs	ROM_WAIT_STATE_REGS	0x0005 F540	0x0005 F541		
Flash0CtrlRegs	FLASH_CTRL_REGS	0x0005 F800	0x0005 FAFF		
Flash0EccRegs	FLASH_ECC_REGS	0x0005 FB00	0x0005 FB3F		
Flash1CtrlRegs	FLASH_CTRL_REGS	0x0005 FC00	0x0005 FEFF		
Flash1EccRegs	FLASH_ECC_REGS	0x0005 FF00	0x0005 FF3F		

6.3 Device Identification Registers

Table 6-6. Device Identification Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
PARTIDH	0x0005 D00A	2	Device part identification number
			TMS320F28377S 0x00FF 0400
			TMS320F28376S 0x00FE 0400
			TMS320F28375S 0x00FD 0400
			TMS320F28374S 0x00FC 0400
REVID	0x0005 D00C	2	Silicon revision number
			Revision B 0x0000 0002

6.4 Bus Architecture – Peripheral Connectivity

Table 6-7 shows a broad view of the peripheral and configuration register accessibility from each bus master. Peripherals within peripheral frames 1 or 2 will all be mapped to the respective secondary master as a group (if SPI is assigned to CPU1.DMA, then McBSP is also assigned to CPU1.DMA).

Table 6-7. Bus Master Peripheral Access

PERIPHERALS (BY BUS ACCESS TYPE)	CPU1.DMA	CPU1.CLA1	CPU1
Peripheral Frame 1: • ePWM/HRPWM • SDFM • eCAP ⁽¹⁾ • eQEP ⁽¹⁾ • CMPSS ⁽¹⁾ • DAC ⁽¹⁾	Y	Y	Y
Peripheral Frame 2: • SPI • McBSP • uPP ⁽¹⁾	Y	Y	Y
SCI			Y
I ² C			Y
CAN			Y
ADC Configuration		Y	Y
EMIF1	Y		Y
EMIF2		Y	Y
USB and USB RAM	Y		Y
Device Capability, Peripheral Reset, Peripheral CPU Select			Y
GPIO Pin Mapping and Configuration			Y
Analog System Control			Y
uPP Message RAMs		Y	Y
Reset Configuration			Y
Clock and PLL Configuration			Y
System Configuration (WD, NMIWD, LPM, Peripheral Clock Gating)			Y
Flash Configuration			Y
CPU Timers			Y
DMA and CLA Trigger Source Select			Y
GPIO Data ⁽²⁾		Y	Y
ADC Results	Y	Y	Y

(1) These modules are on a Peripheral Frame with DMA access; however, they do not support DMA transfers.

(2) The GPIO Data Registers are unique for each CPU1 and CPU1.CLAX. When the GPIO Pin Mapping Register is configured to assign a GPIO to a particular master, the respective GPIO Data Register will control the GPIO. See the "General-Purpose Input/Output (GPIO)" chapter of the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual* ([SPRUHX5](#)) for more details.

6.5 CPU and System Control

6.5.1 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide* ([SPRU430](#)).

6.5.1.1 Floating-Point Unit

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the repeat block register, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information, see the *TMS320C28x Extended Instruction Sets Reference Guide* ([SPRUHS1](#)).

6.5.1.2 Trigonometric Math Unit

The TMU extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in [Table 6-8](#).

Table 6-8. TMU Supported Instructions

INSTRUCTIONS	C EQUIVALENT OPERATION	PIPELINE CYCLES
MPY2PIF32 RaH,RbH	$a = b * 2\pi$	2/3
DIV2PIF32 RaH,RbH	$a = b / 2\pi$	2/3
DIVF32 RaH,RbH,RcH	$a = b/c$	5
SQRTF32 RaH,RbH	$a = \text{sqrt}(b)$	5
SINPUF32 RaH,RbH	$a = \sin(b*2\pi)$	4
COSPUF32 RaH,RbH	$a = \cos(b*2\pi)$	4
ATANPUF32 RaH,RbH	$a = \text{atan}(b)/2\pi$	4
QUADF32 RaH,RbH,RcH,RdH	Operation to assist in calculating ATANPU2	5

No changes have been made to existing instructions, pipeline or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out their operations. A detailed explanation of the workings of the FPU can be found in the *TMS320C28x Extended Instruction Sets Reference Guide* ([SPRUHS1](#)).

6.5.1.3 Viterbi, Complex Math, and CRC Unit II

The VCU-II is the second-generation Viterbi, Complex Math, and CRC extension to the C28x CPU. The VCU-II extends the capabilities of the C28x CPU by adding registers and instructions to accelerate the performance of Fast Fourier Transforms (FFTs) and communications-based algorithms. The C28x+VCU-II supports the following algorithm types:

- **Viterbi Decoding**

Viterbi decoding is commonly used in baseband communications applications. The Viterbi decode algorithm consists of three main parts: branch metric calculations, compare-select (Viterbi butterfly), and a traceback operation. [Table 6-9](#) shows a summary of the VCU performance for each of these operations.

Table 6-9. Viterbi Decode Performance

VITERBI OPERATION	VCU CYCLES
Branch Metric Calculation (code rate = 1/2)	1
Branch Metric Calculation (code rate = 1/3)	2p
Viterbi Butterfly (add-compare-select)	2 ⁽¹⁾
Traceback per Stage	3 ⁽²⁾

(1) C28x CPU takes 15 cycles per butterfly.

(2) C28x CPU takes 22 cycles per stage.

- **Cyclic Redundancy Check**

Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCU can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCU can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

- **Complex Math**

Complex math is used in many applications, a few of which are:

- Fast Fourier Transform

The complex FFT is used in spread spectrum communications, as well as in many signal processing algorithms.

- Complex filters

Complex filters improve data reliability, transmission distance, and power efficiency. The C28x+VCU can perform a complex I and Q multiply with coefficients (four multiplies) in a single cycle. In addition, the C28x+VCU can read/write the real and imaginary parts of 16-bit complex data to memory in a single cycle.

[Table 6-10](#) shows a summary of the VCU operations enabled by the VCU.

Table 6-10. Complex Math Performance

COMPLEX MATH OPERATION	VCU CYCLES	NOTES
Add or Subtract	1	32 +/- 32 = 32-bit (Useful for filters)
Add or Subtract	1	16 +/- 32 = 15-bit (Useful for FFT)
Multiply	2p	16 x 16 = 32-bit
Multiply and Accumulate	2p	32 + 32 = 32-bit, 16 x 16 = 32-bit
RPT MAC	2p+N	Repeat MAC. Single cycle after the first operation.

For more information, see the *TMS320C28x Extended Instruction Sets Reference Guide* ([SPRUHS1](#)).

6.5.2 Control Law Accelerator

The CLA is an independent single-precision (32-bit) floating-point unit processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks can be specified. Each task is started by software or a peripheral such as the ADC, ePWM, eCAP, eQEP, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes, the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers, ePWM, eCAP, eQEP, Comparator and DAC registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

Figure 6-2 shows the CLA block diagram.

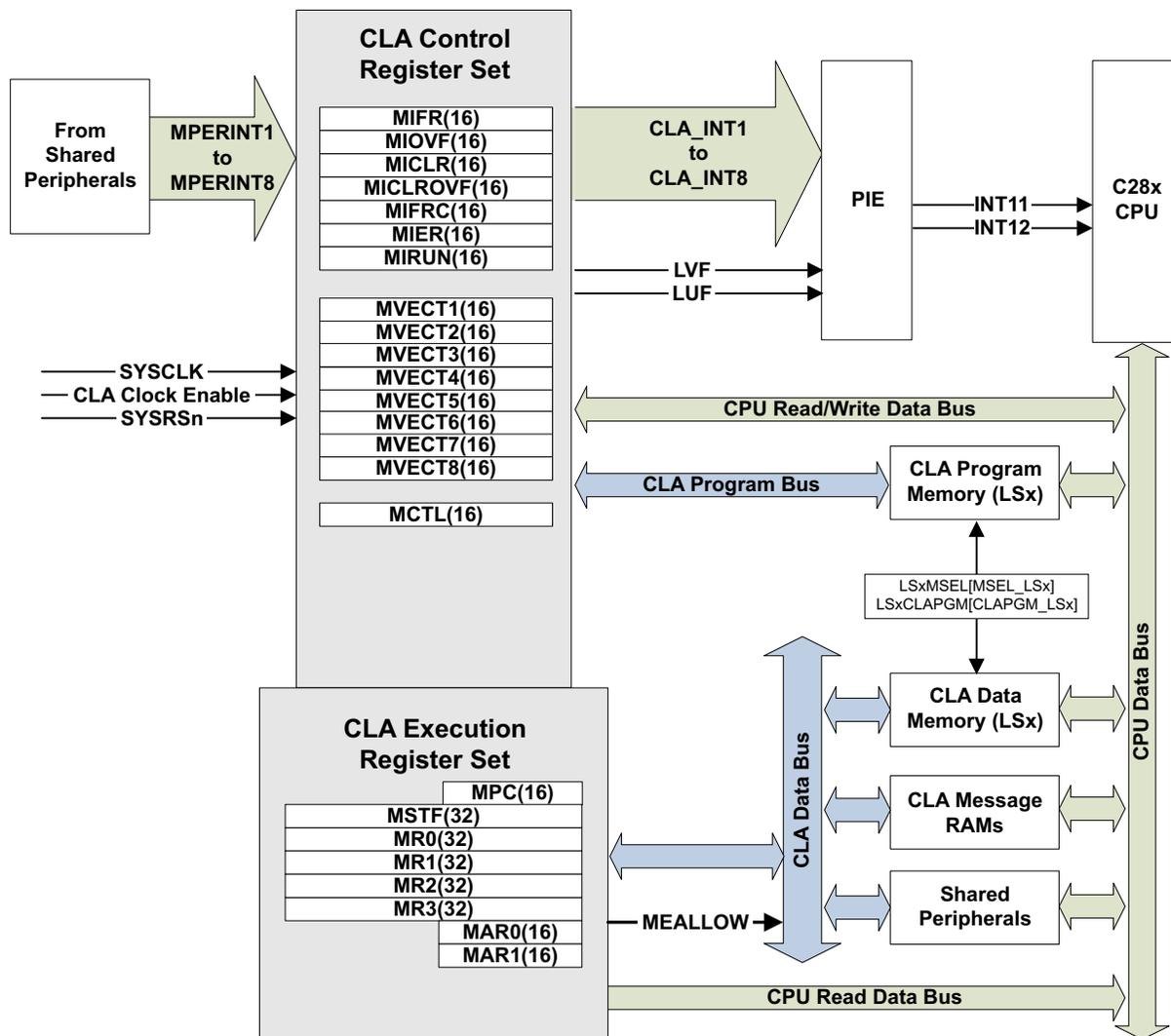


Figure 6-2. CLA Block Diagram

ADVANCE INFORMATION

6.5.3 Direct Memory Access

The CPU has its own 6-channel DMA module. The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing.

The DMA module is an event-based machine, meaning it requires a peripheral or software trigger to start a DMA transfer. Although it can be made into a periodic time-driven machine by configuring a timer as the interrupt trigger source, there is no mechanism within the module itself to start memory transfers periodically. The interrupt trigger source for each of the six DMA channels can be configured separately and each channel contains its own independent PIE interrupt to let the CPU know when a DMA transfer has either started or completed. Five of the six channels are exactly the same, while Channel 1 has the ability to be configured at a higher priority than the others.

DMA features include:

- 6 channels with independent PIE interrupts
- Peripheral interrupt trigger sources
 - ADC interrupts and EVT signals
 - Multichannel buffered serial port transmit and receive
 - External interrupts
 - CPU timers
 - EPWMxSOC signals
 - SPIx transmit and receive
 - USBx transmit and receive
 - Sigma Delta Filter Module
 - Software trigger
- Data sources and destinations:
 - GSx RAM
 - USB RAM
 - ADC result registers
 - ePWMx
 - SPI
 - McBSP
 - EMIF
- Word Size: 16-bit or 32-bit (SPI and McBSP limited to 16-bit)
- Throughput: 4 cycles/word (without arbitration)

Figure 6-3 shows a device-level block diagram of the DMA.

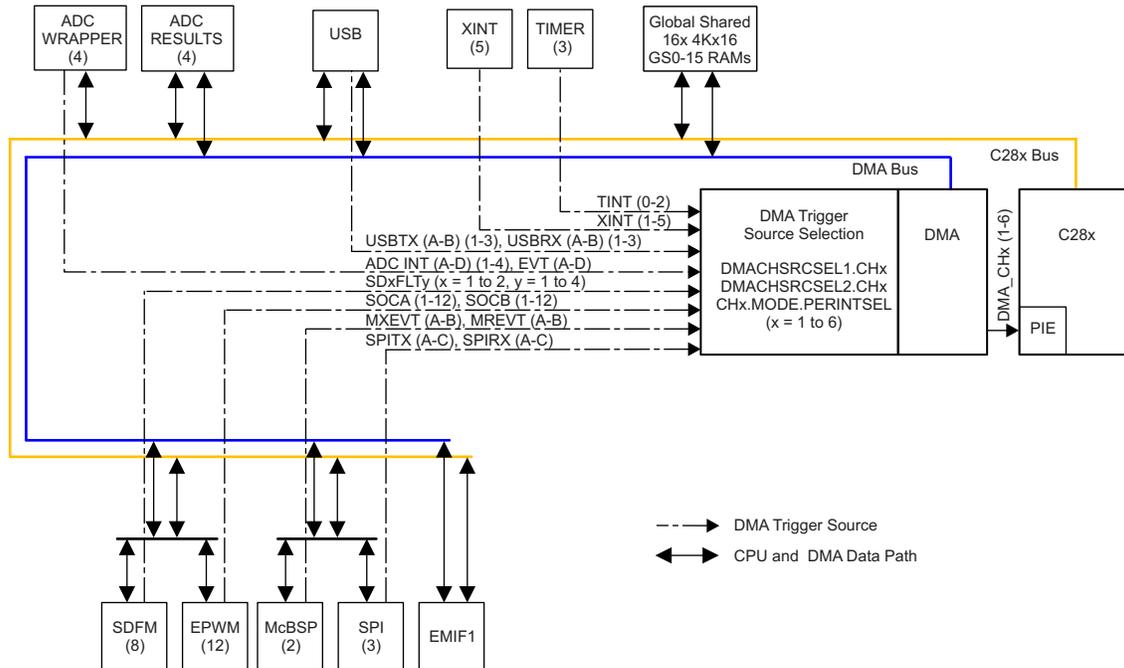


Figure 6-3. DMA Block Diagram

6.5.4 Boot ROM and Peripheral Booting

The device boot ROM is factory-programmed with bootloading software. The device boot ROM is executed each time the device comes out of reset. Users can configure the device to boot to flash (using GET mode) or choose to boot the device through one of the bootable peripherals by configuring the boot mode GPIO pins.

Table 6-11 shows the possible boot modes supported on the device. The default boot mode pins are GPIO72 (boot mode pin 1) and GPIO 84 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming user-configurable Dual Code Security Module (DCSM) OTP locations. This is recommended only for cases in which the factory default boot mode pins do not fit into the customer design. More details on the locations to be programmed is available in the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual (SPRUHX5)*.

Table 6-11. Device Boot Mode – Decoded by CPU1

MODE NO.	CPU1 BOOT MODE	$\overline{\text{TRST}}$	GPIO72 (BOOT MODE PIN 1)	GPIO84 (BOOT MODE PIN 0)
0	Parallel IO	0	0	0
1	SCI Mode	0	0	1
2	Wait Boot Mode	0	1	0
3	Get Mode	0	1	1
4-7	EMU Boot Mode (Emulator Connected)	1	X	X

6.5.4.1 EMU Boot or Emulation Boot

The CPU enters this boot when it detects that $\overline{\text{TRST}}$ is HIGH (in other words, when an emulator/debugger is connected). In this mode, the user can program the EMUBOOTCTRL register (at location 0xD00) to instruct the device on how to boot. If the contents of the EMUBOOTCTRL locations are invalid, then the device would default into WAIT Boot mode. The emulation boot allows users to verify the device boot before programming the boot mode into OTP.

6.5.4.2 WAIT Boot Mode

The device in this boot mode loops in the boot ROM. This mode is useful if users want to connect a debugger on a secure device or if users do not want the device to execute an application in flash yet.

6.5.4.3 Get Mode

The default behavior of Get mode is boot-to-flash. This behavior can be changed by programming the Zx-OTPBOOTCTRL locations in user configurable DCSM OTP. The user configurable DCSM OTP on this device is divided in to two secure zones: Z1 and Z2. The Get mode function in boot ROM first checks if a valid OTPBOOTCTRL value is programmed in Z1. If the answer is yes, then the device boots as per the Z1-OTPBOOTCTRL location. The Z2-OTPBOOTCTRL location is read and decodes only if Z1-OTPBOOTCTRL is invalid or not programmed. If either Zx-OTPBOOTCTRL location is not programmed, then the device defaults to factory default operation, which is to use factory default boot mode pins to boot to flash if the boot mode pins are set to GET MODE. Users can choose the device through which to boot—SPI, I2C, CAN and USB—by programming proper values into the user configurable DCSM OTP. More details on this can be found in the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual* ([SPRUHX5](#)).

6.5.4.4 Peripheral Pins used by Bootloaders

Table 6-12 shows the GPIO pins used by each peripheral bootloader. This device supports two sets of GPIOs for each mode, as shown in Table 6-12.

Table 6-12. GPIO Pins Used by Each Peripheral Bootloader

BOOTLOADER	GPIO PINS	NOTES
SCI-Boot0	SCITXDA: GPIO84 SCIRXDA: GPIO85	SCIA Boot IO option 1 (default SCI option when chosen through Boot Mode GPIOs)
SCI-Boot1	SCITXDA: GPIO28 SCIRXDA: GPIO29	SCIA Boot option 2 – with alternate IOs.
Parallel Boot	D0 – GPIO65 D1 – GPIO64 D2 – GPIO58 D3 – GPIO59 D4 – GPIO60 D5 – GPIO61 D6 – GPIO62 D7 – GPIO63 HOST_CTRL – GPIO70 DSP_CTRL – GPIO69	
CAN-Boot0	CANRXA: GPIO70 CANTXA: GPIO71	CAN-A Boot -IO Option 1
CAN-Boot1	CANRXA: GPIO62 CANTXA: GPIO63	CAN-A Boot -IO option 2
I2C-Boot0	SDAA: GPIO91 SCLA: GPIO92	I2CA Boot- IO option 1
I2C-Boot1	SDAA: GPIO32 SCLA: GPIO33	I2CA Boot- IO option 2
SPI-Boot0	SPISIMOA - GPIO58 SPISOMIA - GPIO59 SPICLKA - GPIO60 SPISTEA - GPIO61	SPIA Boot- IO Option 1
SPI-Boot1	SPISIMOA – GPIO16 SPISOMIA – GPIO17 SPICLKA – GPIO18 SPISTEA – GPIO19	SPIA Boot - IO Option 2
USB Boot	USB0DM - GPIO42 USB0DP - GPIO43	USB Boot implements USB custom DFU device type

6.5.5 Memory

6.5.5.1 Dedicated RAM (Mx and Dx RAM)

The CPU subsystem has four dedicated ECC-capable RAM blocks: M0, M1, D0, and D1. M0/M1 memories are small non-secure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them). D0/D1 memories are secure blocks and also have the access-protection feature (CPU write/CPU fetch protection).

6.5.5.2 Local Shared RAM (LSx RAM)

RAM blocks which are dedicated to each subsystem and are accessible to its CPU and CLA only, are called local shared RAMs (LSx RAMs).

All LSx RAM blocks have parity. These memories are secure and have the access protection (CPU write/CPU fetch) feature.

By default, these memories are dedicated to the CPU only, and the user could choose to share these memories with the CLA by configuring the MSEL_LSx bit field in the LSxMSEL registers appropriately.

**Table 6-13. Master Access for LSx RAM
(With Assumption That all Other Access Protections are Disabled)**

MSEL_LSx	CLAPGM_LSx	CPU ALLOWED ACCESS	CLA1 ALLOWED ACCESS	COMMENT
00	X	All	–	LSx memory is configured as CPU dedicated RAM.
01	0	All	Data Read Data Write	LSx memory is shared between CPU and CLA1.
01	1	Emulation Read Emulation Write	Fetch Only	LSx memory is CLA1 program memory.

6.5.5.3 Global Shared RAM (GSx RAM)

RAM blocks which are accessible from both the CPU and DMA are called global shared RAMs (GSx RAMs). Both the CPU and DMA have full read and write access to these memories.

The GSx RAMs have access protection (CPU write/CPU fetch/DMA write).

6.5.5.4 CLA Message RAM (CLA MSGRAM)

These RAM blocks are be used to share data between the CPU and CLA. The CLA has read and write access to the "CLA to CPU MSGRAM". The CPU has read and write access to the "CPU to CLA MSGRAM". The CPU and CLA both have read access to both MSGRAMs.

This RAM has parity.

6.5.6 Dual Code Security Module

The DCSM prevents access to on-chip secure memories. The term "secure" means access to secure memories and resources is blocked. The term "unsecure" means access is allowed; for example, through a debugging tool such as Code Composer Studio.

The code security mechanism offers protection for two zones, Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both the zones is identical. Each zone has its own dedicated secure resource and allocated secure resource.

The security of each zone is ensured by its own 128-bit password (CSM password). The password for each zone is stored in an OTP memory location based on a zone-specific link pointer. The link pointer value can be changed to program a different set of security settings (including passwords) in OTP. The secure resources available are: OTP memory, CLA, LSx RAM, flash sectors, and secure ROM.

6.5.7 Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presetable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for SYSBIOS. It is connected to INT14 of the CPU. If SYSBIOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- External clock source

6.5.8 Interrupts

Figure 6-4 provides a high-level view of the interrupt architecture.

As shown in Figure 6-4, the devices support five external interrupts (XINT1 to XINT5) that can be mapped onto any of the GPIO pins.

In this device, sixteen ePIE block interrupts are grouped into one CPU interrupt. In total, there are 12 CPU interrupt groups, with 16 interrupts per group.

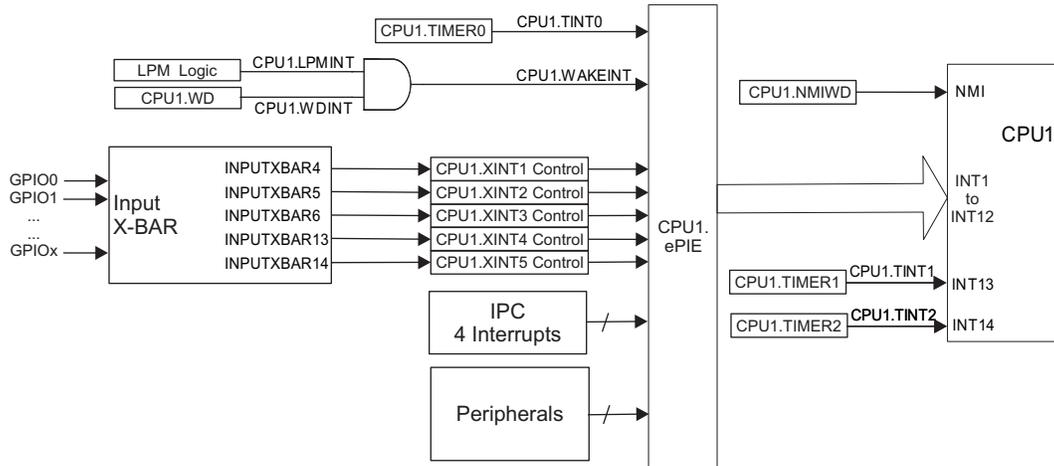


Figure 6-4. External and ePIE Interrupt Sources

6.5.9 Nonmaskable Interrupt Watchdog

The NMI is used to monitor erroneous conditions in the system. The conditions monitored are:

- A missing clock condition
- Uncorrectable memory errors on C28x access to Flash
- Uncorrectable memory errors on C28x, CLA, or DMA access to RAM
- Vector fetch ERROR on the other CPU

If the software does not respond to the enabled latched FAIL condition, then the NMI watchdog will trigger a reset after a preprogrammed time interval.

6.5.10 Watchdog

The watchdog module is the same as the one on previous C2000 devices, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backwards-compatible.

The watchdog is capable of generating either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 6-5 shows the various functional blocks within the watchdog module.

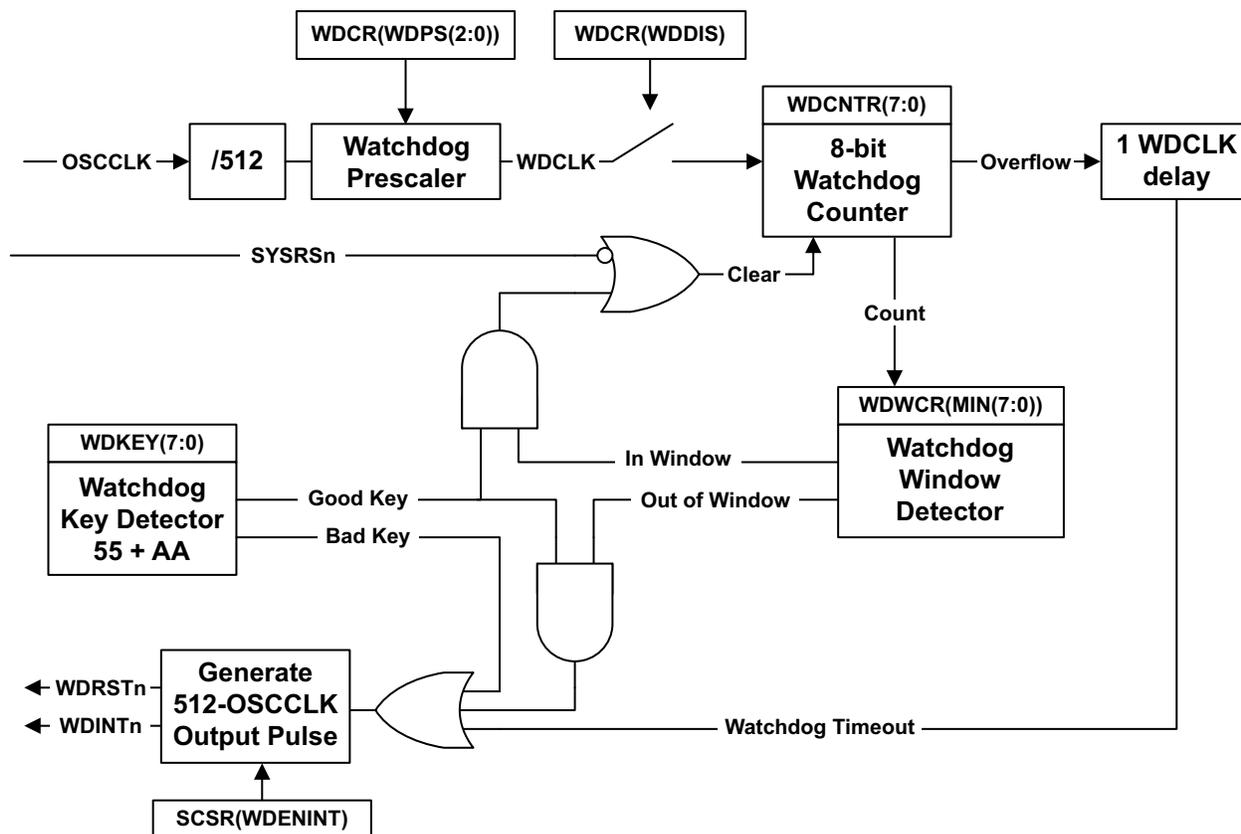


Figure 6-5. Windowed Watchdog

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6.5.11 Low-Power Modes

This device has three clock-gating low-power modes and a special power-gating mode.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the "Low Power Modes" section of the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual (SPRUHX5)*.

6.5.11.1 Clock-Gating Low-Power Modes

IDLE, STANDBY, and HALT modes on this device are similar to those on other C28x devices. [Table 6-14](#) describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 6-14. Effect of Clock-Gating Low-Power Modes on the Device

MODULES/ CLOCK DOMAIN	CPU1 IDLE	CPU1 STANDBY	HALT
CPU1.CLKIN	Active	Gated	Gated
CPU1.SYSCLK	Active	Gated	Gated
CPU1.CPUCLK	Gated	Gated	Gated
Clock to modules Connected to PERx.SYSCLK	Active	Gated	Gated
WD1CLK	Active	Active	Gated if CLKSRCCTL1.WDHALTI = 0
WD2CLK	Active	Active	Gated
AUXPLLCLK	Active	Active	Gated
PLL	Powered	Powered	Powered-Down
INTOSC1	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
INTOSC2	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
Flash	Powered	Powered	Software-Controlled
X1,X2 OSC	Powered	Powered	Powered-Down

6.5.11.2 Power-Gating Low-Power Modes

HIBERNATE mode is the lowest power mode on this device. It is a global low-power mode that gates the supply voltages to most of the system. HIBERNATE is essentially a controlled power-down with remote wakeup capability, and can be used to save power during long periods of inactivity. [Table 6-15](#) describes the effects on the system when the HIBERNATE mode is entered.

Table 6-15. Effect of Power-Gating Low-Power Mode on the Device

MODULES/POWER DOMAINS	HIBERNATE
M0 and M1 memories	<ul style="list-style-type: none"> Remain on with memory retention if LPMCR.M0M1MODE = 0x00 Are off when LPMCR.M0M1MODE = 0x01
CPU1, digital peripherals	Powered down
Dx, LSx, GSx memories	Power down, memory contents are lost
IOs	On with output state preserved
Oscillators, PLL, analog peripherals, Flash	Enters Low-Power Mode

6.6 Analog Peripherals

NOTE

For the actual number of each peripheral on a specific device, see [Table 3-1](#).

The analog subsystem consists of:

- Four ADCs with selectable resolution of 16 bits or 12 bits
- Eight comparator subsystems, each containing a 12-bit reference DAC, two comparators, and a digital deglitching filter
- Three 12-bit buffered output DACs

[Figure 6-6](#) shows the Analog Subsystem Block Diagram for the 337-ball ZWT package. [Figure 6-7](#) shows the Analog Subsystem Block Diagram for the 176-pin PTP package. [Figure 6-8](#) shows the Analog Subsystem Block Diagram for the 100-pin PZP package.

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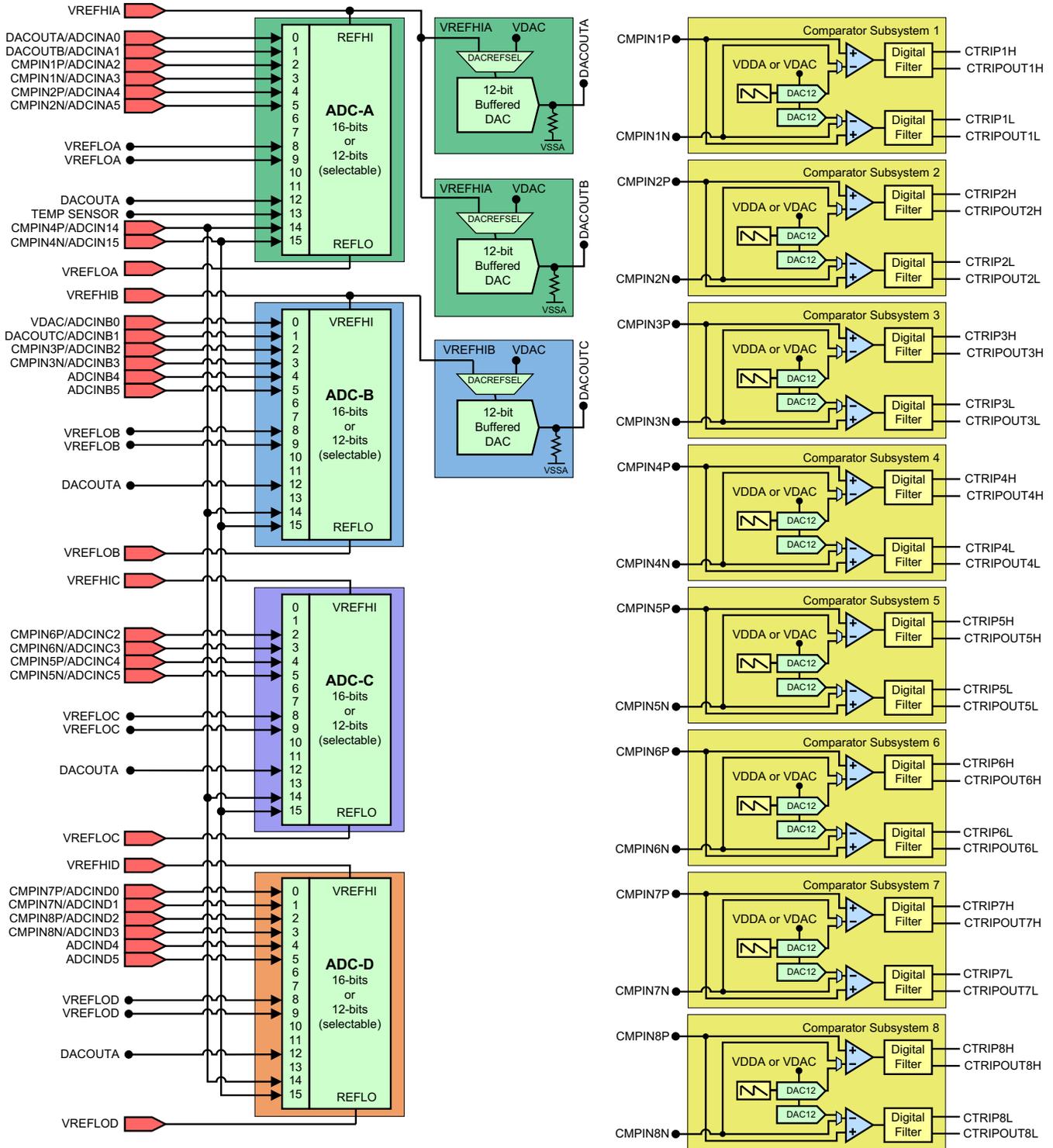


Figure 6-6. Analog Subsystem Block Diagram (337-Ball ZWT)

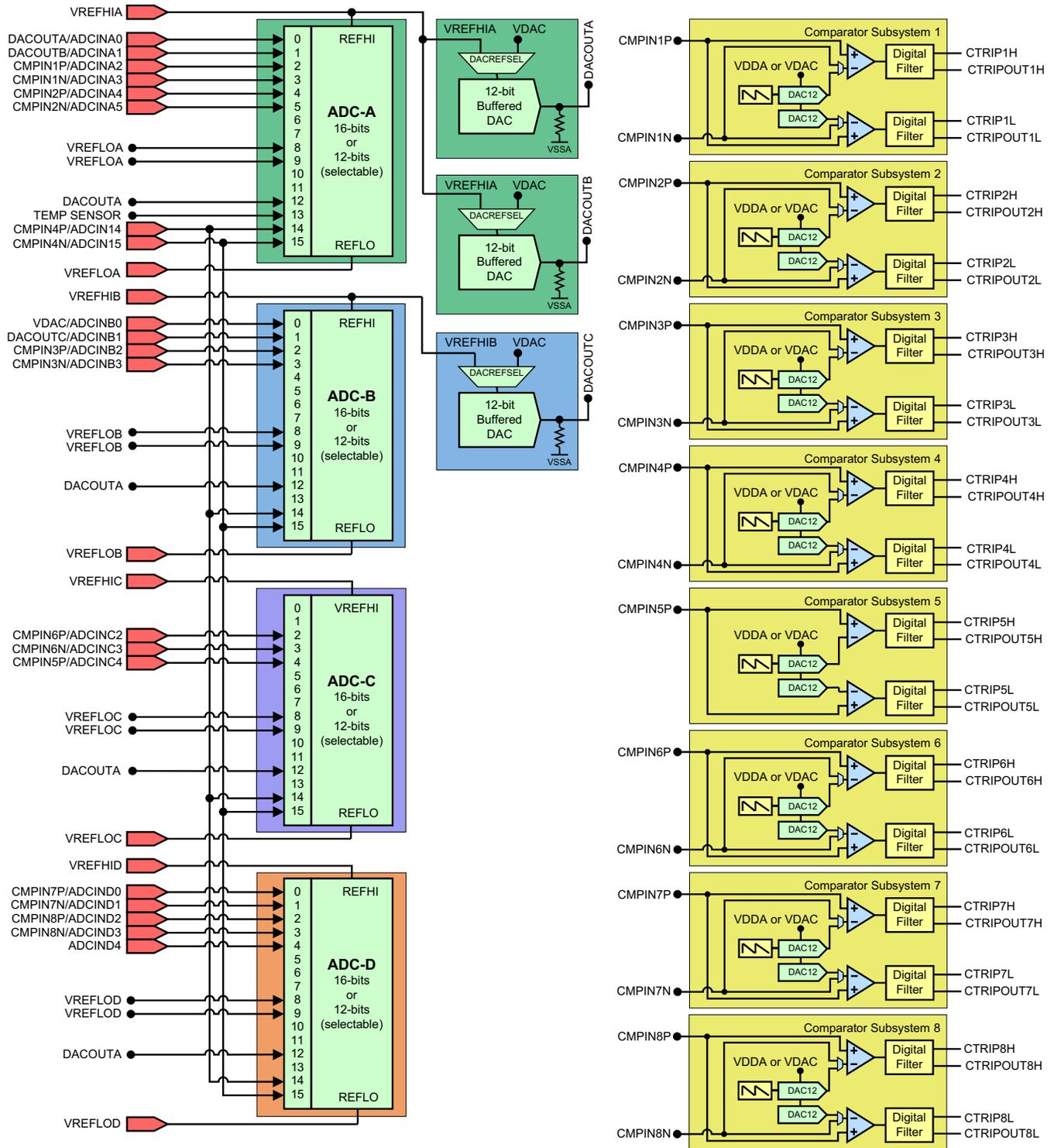


Figure 6-7. Analog Subsystem Block Diagram (176-Pin PTP)

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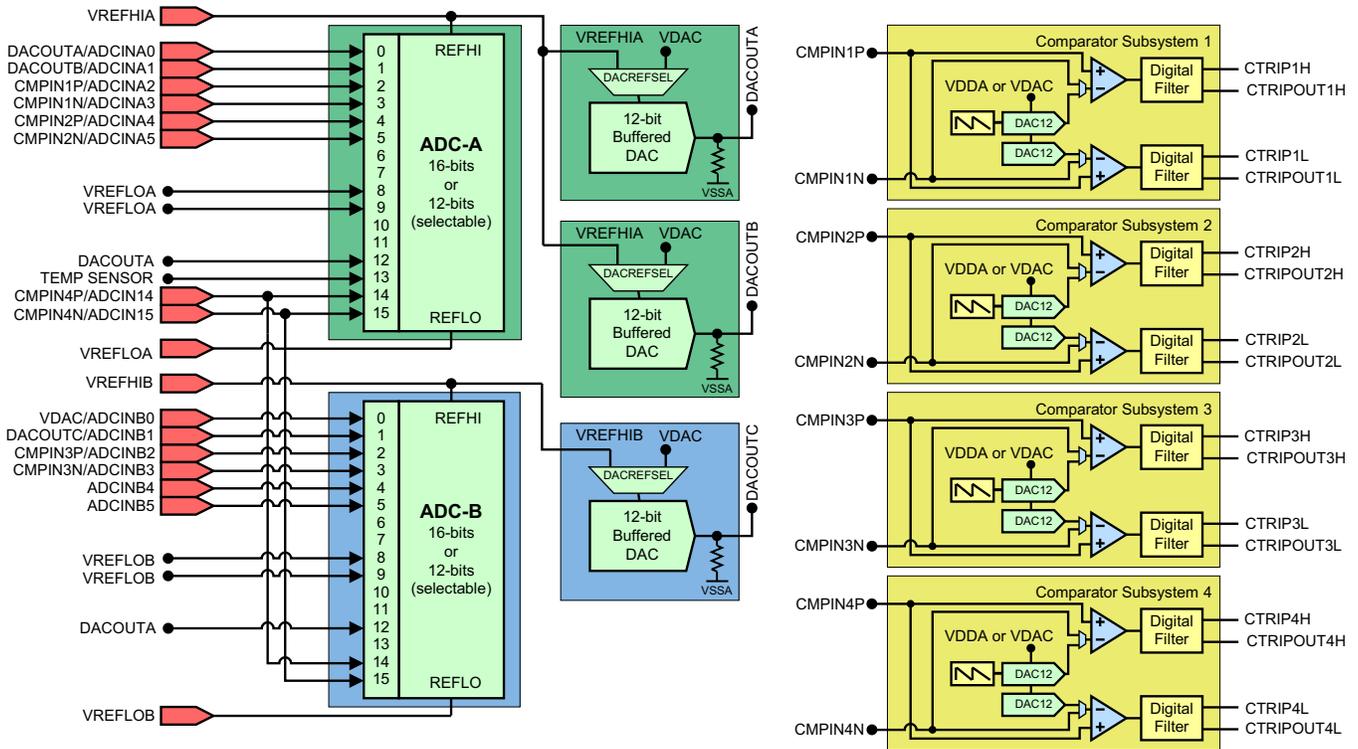


Figure 6-8. Analog Subsystem Block Diagram (100-Pin PZP)

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6.6.1 Analog-to-Digital Converter

The ADCs on this device are successive approximation (SAR) style ADCs with selectable resolution of either 16 bits or 12 bits. There are multiple ADC modules, allowing simultaneous sampling or independent operation. The ADC wrapper is start-of-conversion (SOC) based [see the "SOC Principle of Operation" section of the *TMS320F2837xS Delfino Microcontrollers Technical Reference Manual* ([SPRUHX5](#))].

Each ADC has the following features:

- Selectable resolution of 16 bits or 12 bits
- Ratiometric external reference set by V_{REFHI} and V_{REFLO}
- Differential signal conversions
- Single-ended signal conversions (12-bit mode only)
- Input multiplexer with up to 16 channels (single-ended) or 8 channels (differential)
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
 - Software immediate start
 - All ePWMs
 - GPIO XINT2
 - CPU timers
 - ADCINT1 or 2
- Four flexible PIE interrupts
- Burst mode
- Four post-processing blocks, each with:
 - Saturating offset calibration
 - Error from setpoint calculation
 - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
 - Trigger-to-sample delay capture

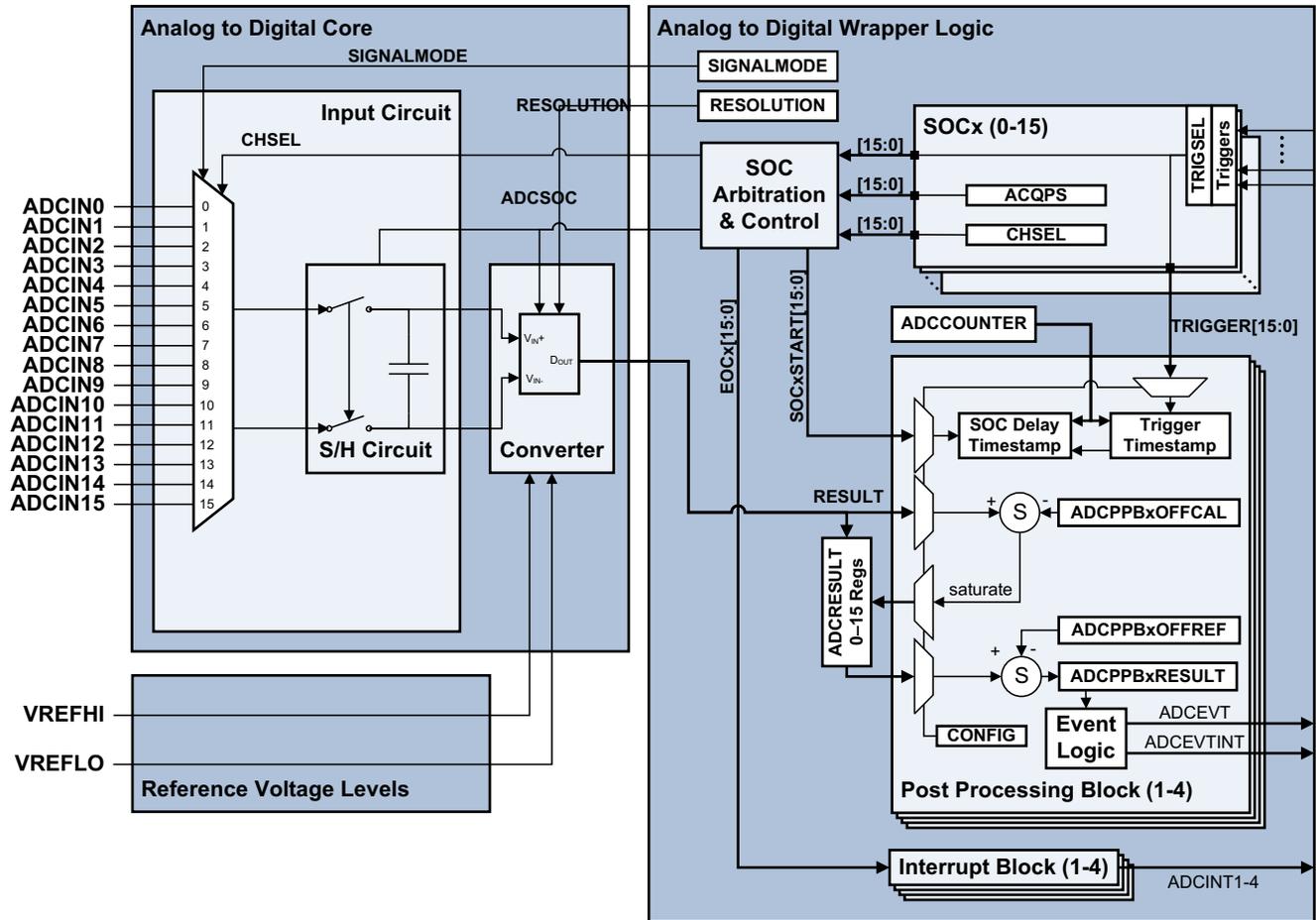


Figure 6-9. ADC Module Block Diagram

6.6.2 Buffered Digital-to-Analog Converter

The buffered DAC module consists of an internal reference DAC and an analog output buffer that is capable of driving an external load. An integrated pulldown resistor on the DAC output helps to provide a known pin voltage when the output buffer is disabled. This pulldown resistor cannot be disabled and remains as a passive component on the pin, even for other shared pin mux functions. Software writes to the DAC value register can take effect immediately or can be synchronized with PWMSYNC events.

Each Buffered DAC has the following features:

- 12-bit programmable internal DAC
- Selectable reference voltage
- Pulldown resistor on output
- Ability to synchronize with PWMSYNC

The block diagram for the buffered DAC is shown in Figure 6-10.

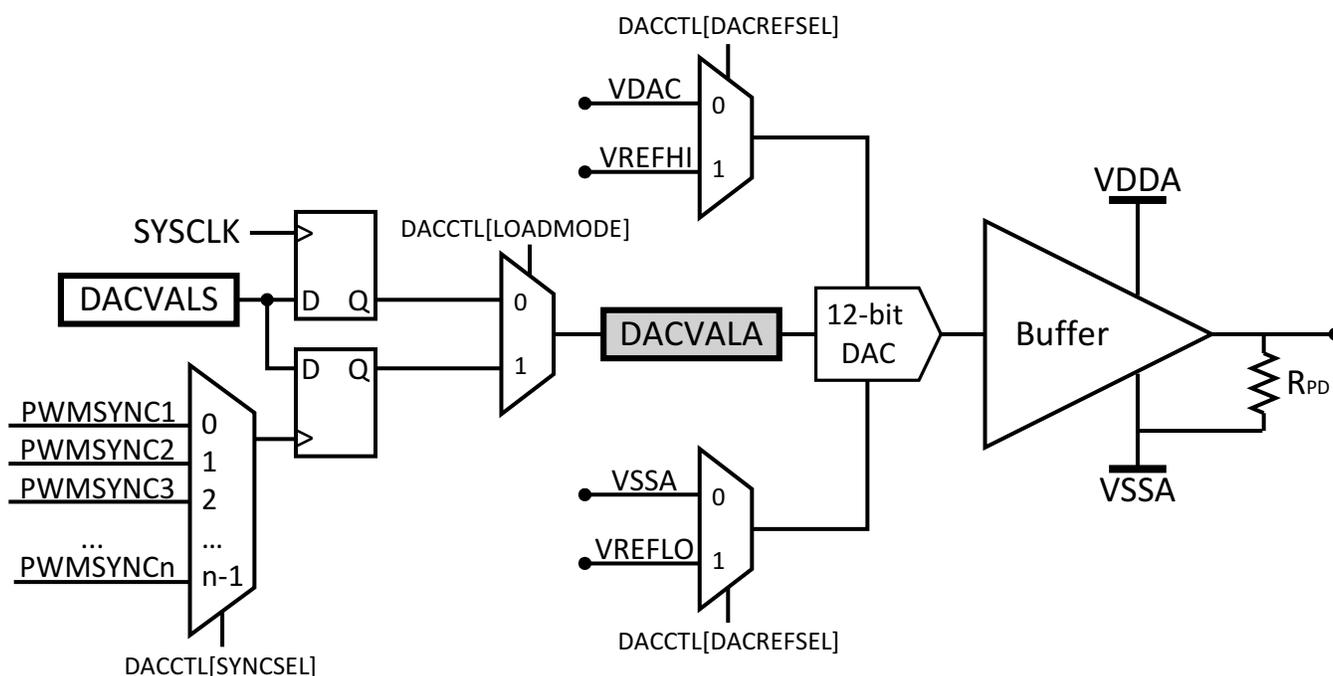


Figure 6-10. DAC Module Block Diagram

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6.6.3 Comparator Subsystem

Each CMPSS module includes two sets of comparators, internal voltage reference DACs, digital glitch filters, and ramp generator logic. There are two inputs, CMPINxP and CMPINxN. Each of these will be internally connected to an ADCIN pin. The CMPINxP pin is always connected to the positive input of the CMPSS comparators. CMPINxN can be used instead of the DAC output to drive the negative comparator inputs. There are two comparators, and therefore two outputs from the CMPSS module, which are connected to the input of a digital filter module before being passed on to the Comparator TRIP crossbar and either PWM modules or directly to a GPIO pin. Figure 6-11 shows the CMPSS connectivity on the 337-ball ZWT and 176-pin PTP packages. Figure 6-12 shows CMPSS connectivity on the 100-pin PZP package.

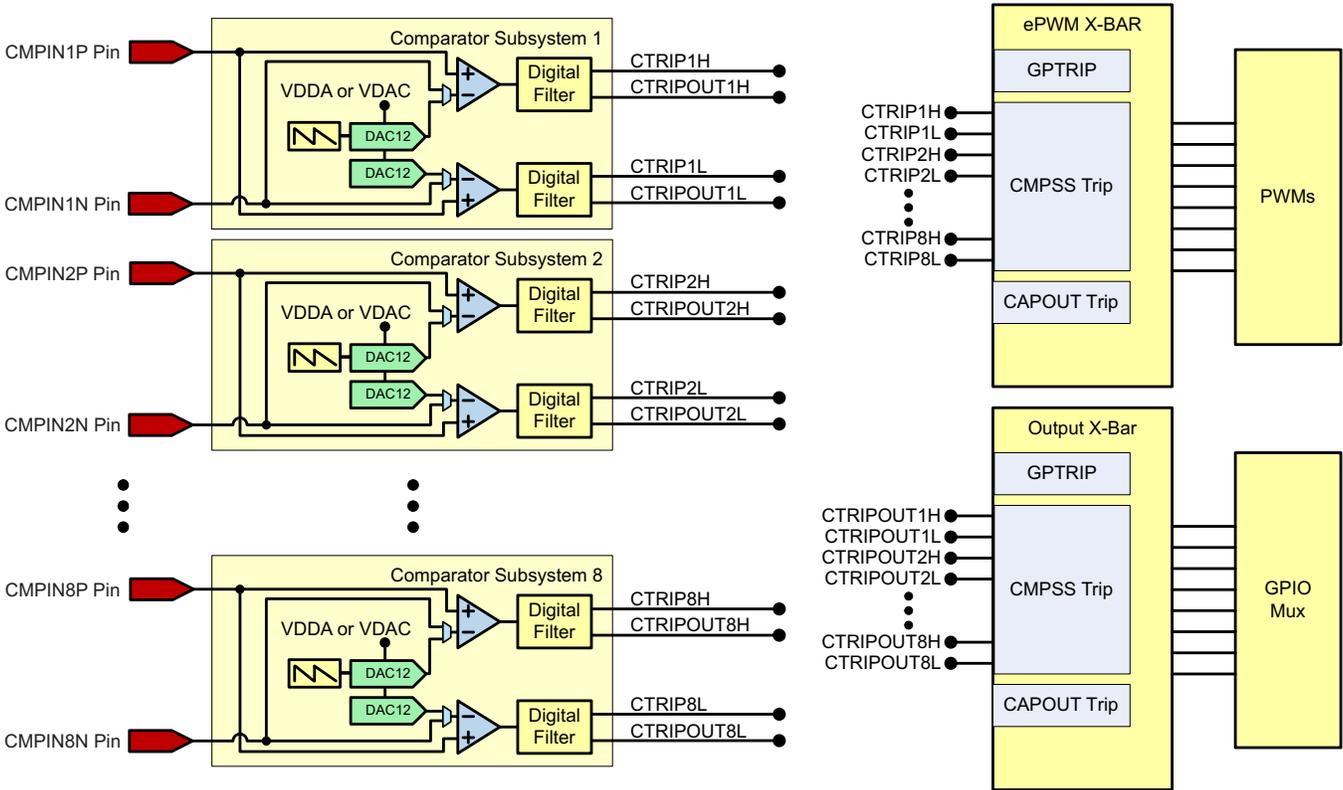


Figure 6-11. CMPSS Connectivity (337-Ball ZWT and 176-Pin PTP)

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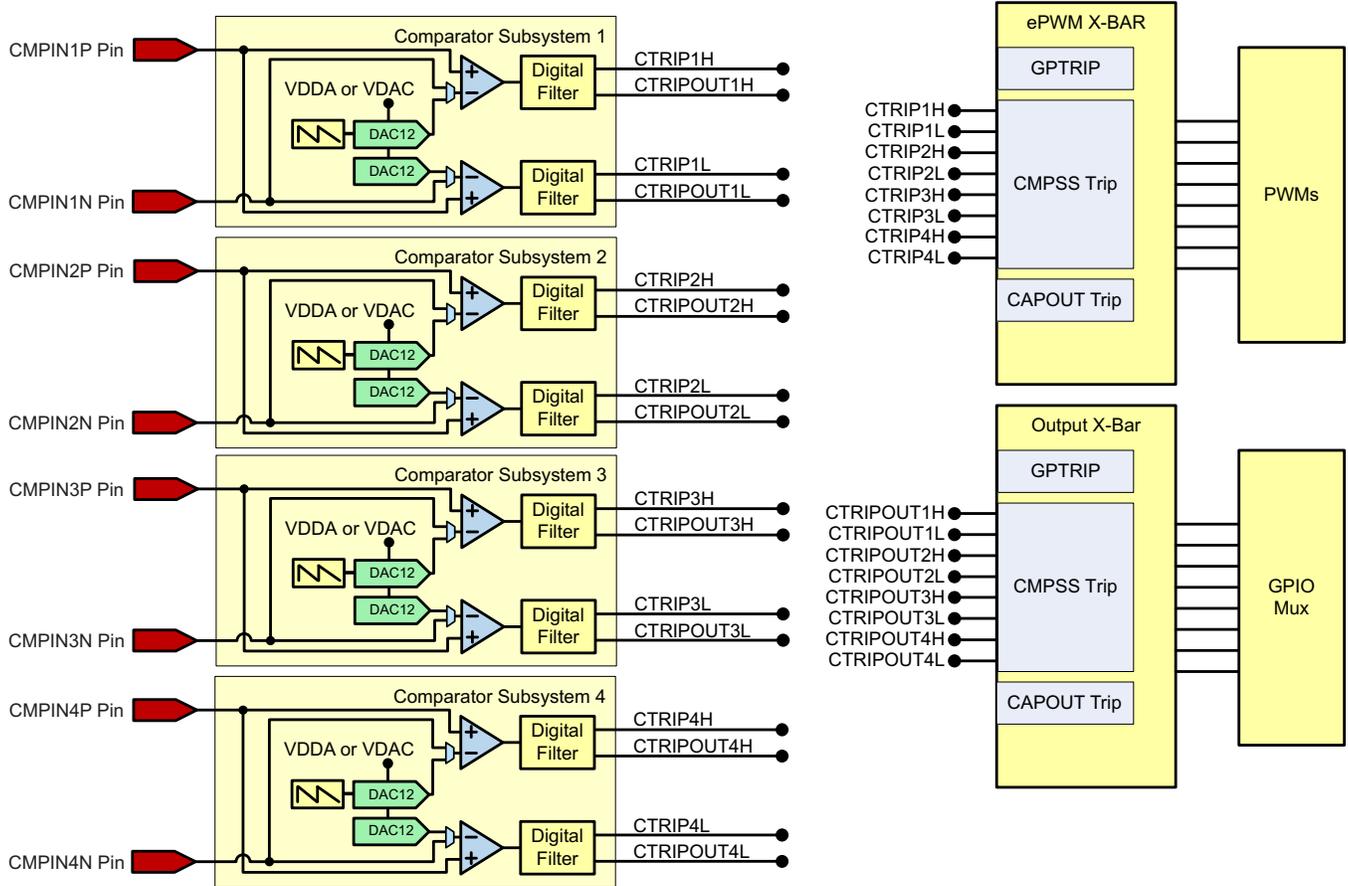


Figure 6-12. CMPSS Connectivity (100-Pin PZP)

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6.7 Control Peripherals

NOTE

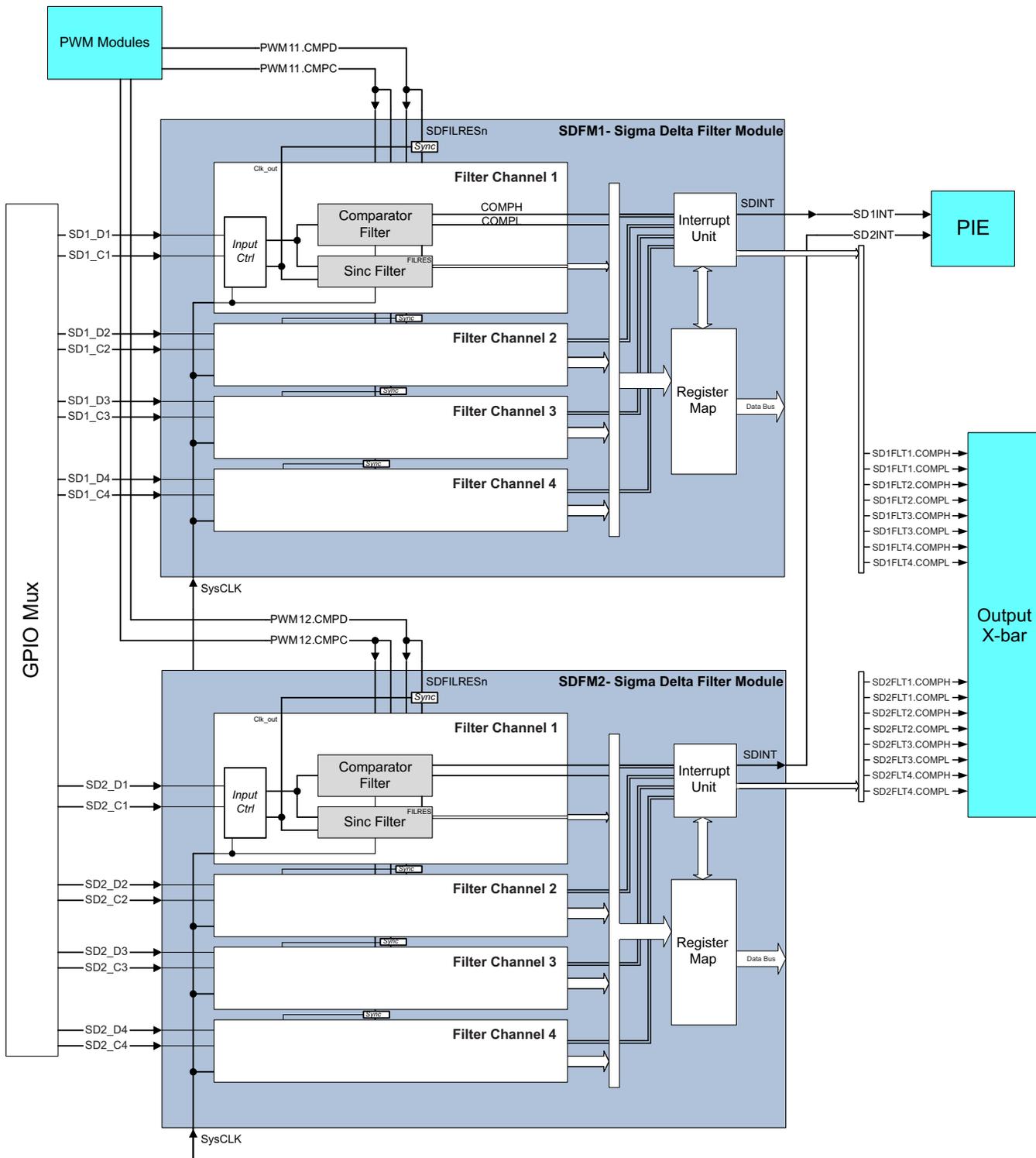
For the actual number of each peripheral on a specific device, see [Table 3-1](#).

6.7.1 Sigma Delta Filter Module

The SDFM is a four-channel digital filter designed specifically for current measurement and resolver position decoding in motor control applications. Each channel can receive an independent sigma-delta ($\Sigma\Delta$) modulated bit stream. The bit streams are processed by four individually programmable digital decimation filters. The filter set includes a fast comparator for immediate digital threshold comparisons for over-current and under-current monitoring. The flexible SDFM also offers a filter-bypass mode to enable data logging, analysis, and customized filtering. [Figure 6-13](#) shows a block diagram of the SDFMs.

SDFM features include:

- Four external pins per SDFM module:
 - Four sigma delta data input pins per SDFM module (SDx_Dy, where x = 1 to 2 and y = 1 to 4)
 - Four sigma delta clock input pins per SDFM module (SDx_Cy, where x = 1 to 2 and y = 1 to 4)
- Four different configurable modulator clock modes:
 - Modulator clock rate equals modulator data rate
 - Modulator clock rate running at half the modulator data rate
 - Modulator data is Manchester encoded. Modulator clock not required.
 - Modulator clock rate is double that of modulator data rate
- Four independent configurable comparator units:
 - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
 - Ability to detect over-value and under-value conditions
 - OSR value for comparator programmable from 1 to 32
- Four independent configurable sinc filter units:
 - Four different filter type selection (Sinc1/Sinc2/Sincfast/Sinc3) options available
 - Ability to bypass filter module
 - OSR value for filter unit programmable from 1 to 256
 - Ability to enable or disable individual filter module
 - Ability to synchronize all four independent filters of a SDFM module using the Master Filter Enable (MFE) bit or the PWM signals.
- Filter data can be 16-bit or 32-bit representation
- PWMs can be used to generate modulator clock for sigma delta modulators



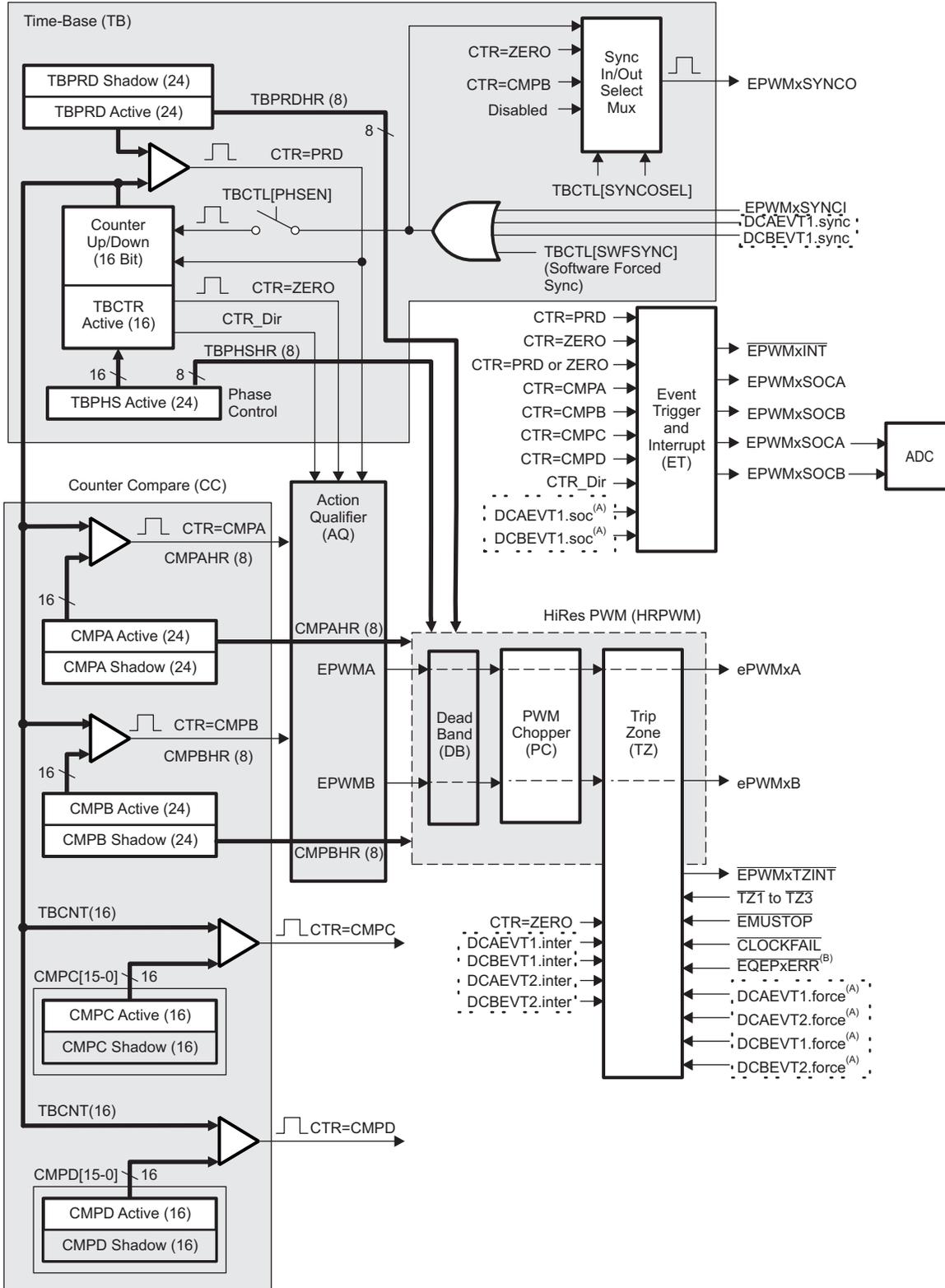
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Figure 6-13. SDFM

6.7.2 Enhanced Pulse Width Modulator

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

[Figure 6-14](#) shows the signal interconnections with the ePWM.



A. These events are generated by the type-4 ePWM digital compare (DC) submodule.

Figure 6-14. ePWM Sub-Modules Showing Critical Internal Signal Interconnections

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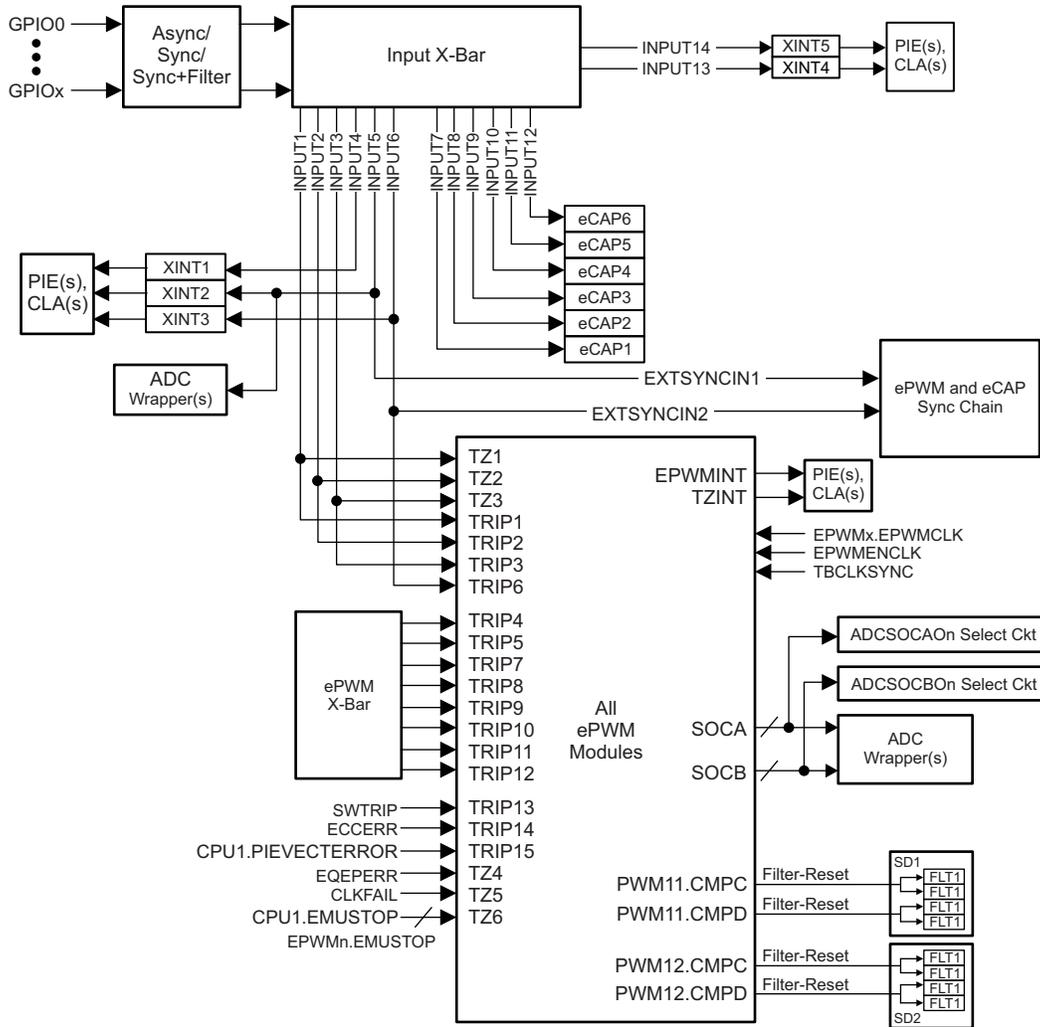


Figure 6-15. ePWM

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6.7.2.1 Control Peripherals Synchronization

The ePWM and eCAP Synchronization Chain allows synchronization between multiple modules for the system. Figure 6-16 shows the Synchronization Chain Architecture.

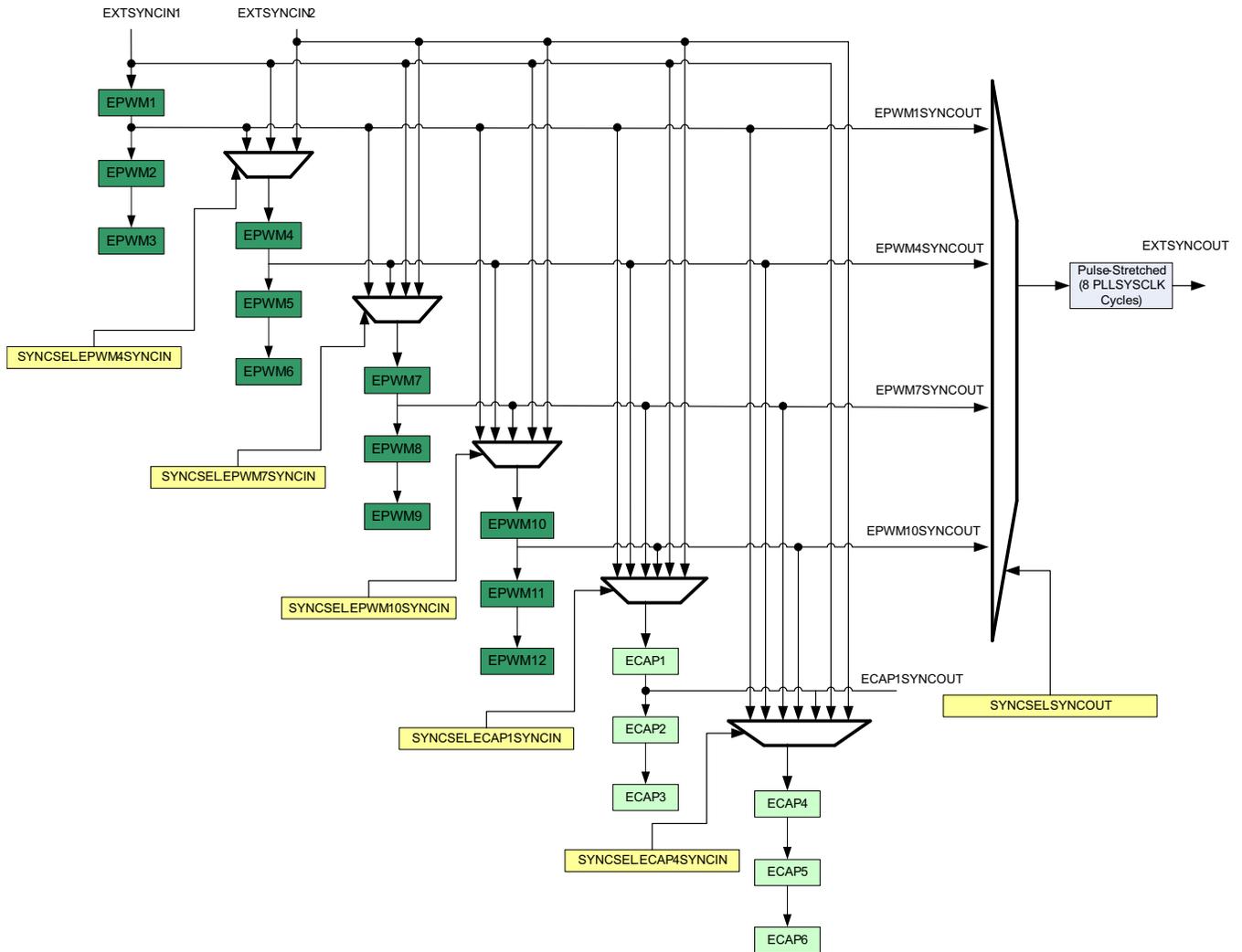


Figure 6-16. Synchronization Chain Architecture

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6.7.3 High-Resolution Pulse Width Modulator

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module there is one HR delay line.

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be utilized in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled via extensions to the Compare A, phase, and period registers of the ePWM module.

NOTE

The minimum HRPWMCLK frequency allowed for HRPWM is 60 MHz.

NOTE

When dual-edge high-resolution is enabled (high-resolution period mode), the PWMxB output is not available for use.

6.7.4 Enhanced Capture

Figure 6-17 shows the block diagram of an eCAP module.

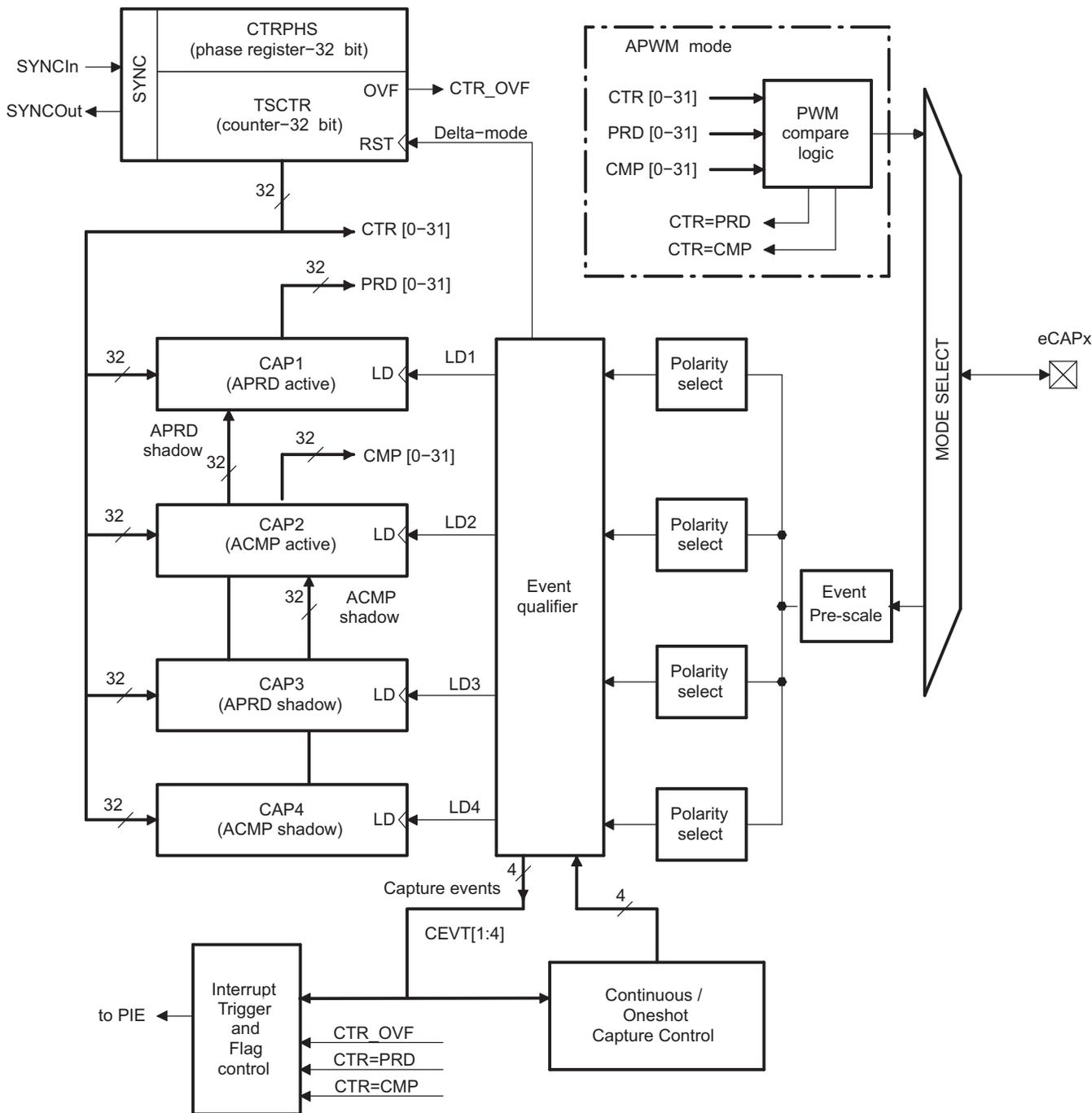


Figure 6-17. eCAP Block Diagram

The eCAP module is clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1–ECAP6) in the PCLKCR3 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

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6.7.5 Enhanced Quadrature Encoder Pulse

Figure 6-18 shows the eQEP block diagram.

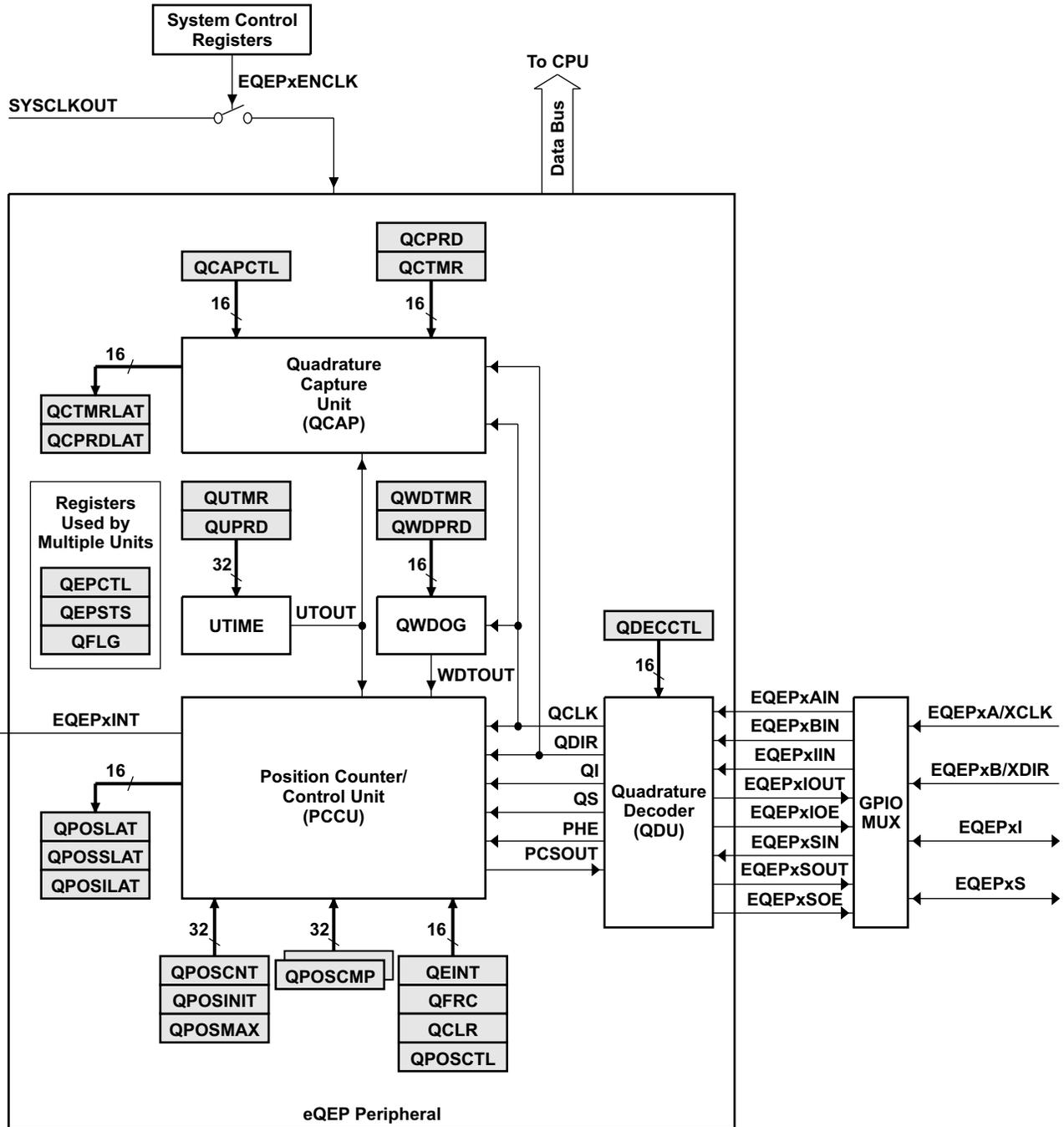


Figure 6-18. eQEP Block Diagram

ADVANCE INFORMATION

6.8 Communications Peripherals

NOTE

For the actual number of each peripheral on a specific device, see [Table 3-1](#).

6.8.1 Serial Peripheral Interface

The SPI is a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the microcontroller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion via devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. The port supports 16-level receive and transmit FIFOs for reducing CPU servicing overhead.

The SPI module features include:

- SPISOMI: SPI slave-output/master-input pin
- SPISIMO: SPI slave-input/master-output pin
- $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: master and slave
- Baud rate: 125 different programmable rates
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
 - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
 - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive-and-transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- 16-level transmit and receive FIFO
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPISTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules
- DMA support
- High-speed mode for up to 40-MHz full-duplex communication

The SPI operates in master or slave mode. The master initiates data transfer by sending the SPICLK signal. For both the slave and the master, data is shifted out of the shift registers on one edge of the SPICLK and latched into the shift register on the opposite SPICLK clock edge. If the CLOCK PHASE bit (SPICLK.3) is high, data is transmitted and received a half-cycle before the SPICLK transition. As a result, both controllers send and receive data simultaneously. The application software determines whether the data is meaningful or dummy data. There are three possible methods for data transmission:

- Master sends data; slave sends dummy data
- Master sends data; slave sends data
- Master sends dummy data; slave sends data

The master can initiate a data transfer at any time because it controls the SPICLK signal. The software, however, determines how the master detects when the slave is ready to broadcast data.

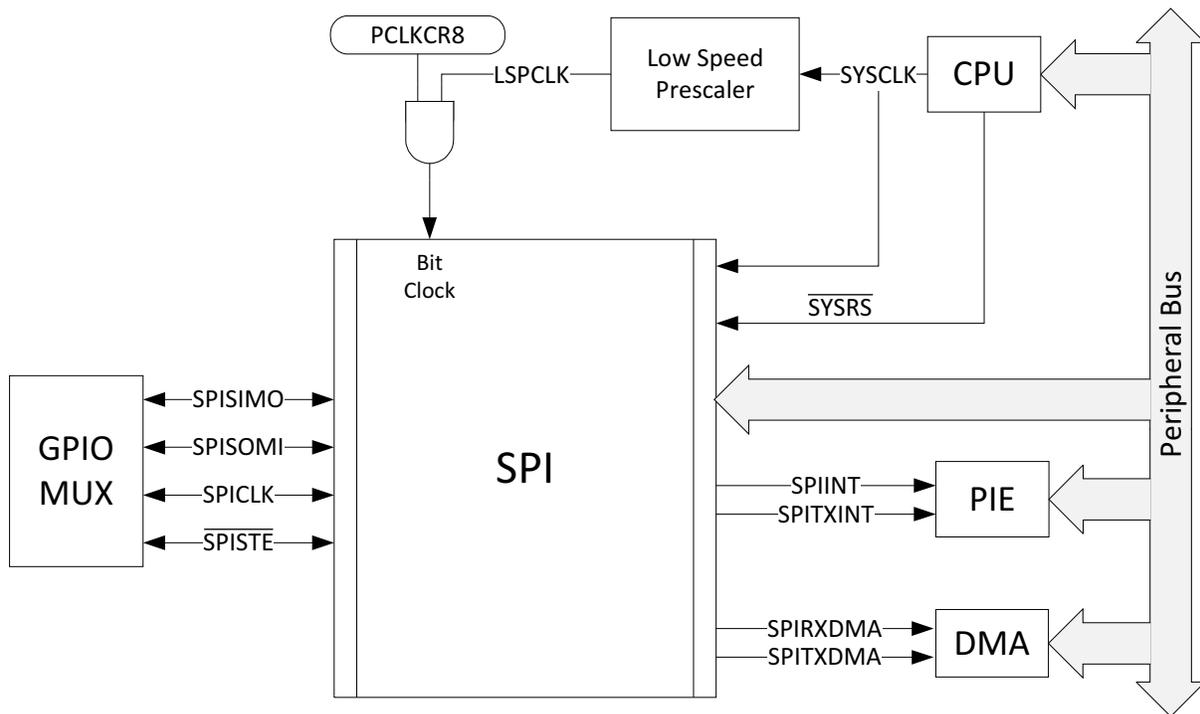


Figure 6-19. SPI

6.8.2 Serial Communications Interface

The SCI is a two-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
 - SCITXD: SCI transmit-output pin
 - SCIRXD: SCI receive-input pin
 - NOTE:** Both pins can be used as GPIO if not used for SCI.
 - Baud rate programmable to 64K different rates
- Data-word format
 - One start bit
 - Data-word length programmable from one to eight bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
 - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
 - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

NOTE

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

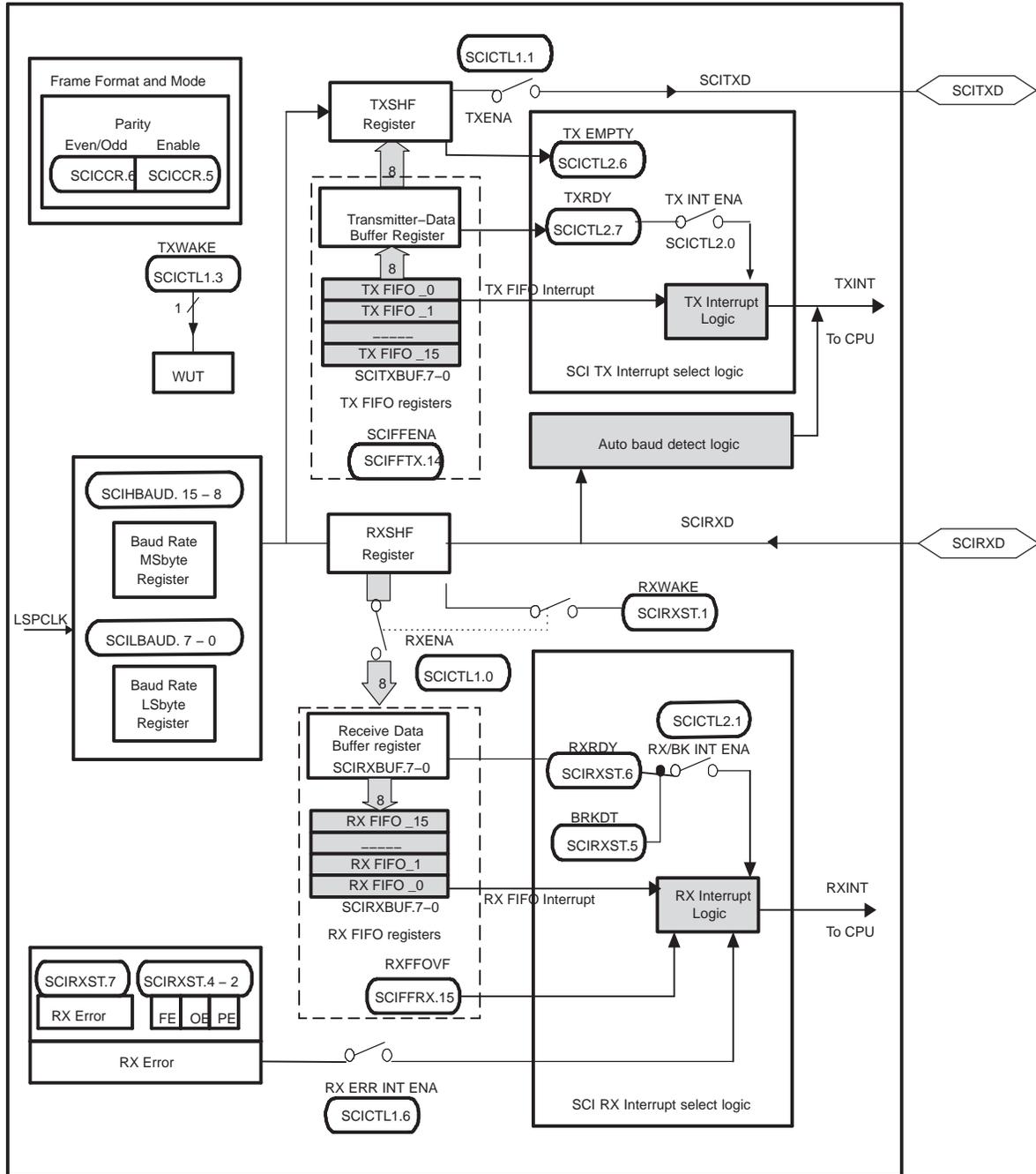


Figure 6-20. SCI Block Diagram

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The major elements used in full-duplex operation include:

- A transmitter (TX) and its major registers:
 - SCITXBUF register – Transmitter Data Buffer register. Contains data (loaded by the CPU) to be transmitted
 - TXSHF register – Transmitter Shift register. Accepts data from the SCITXBUF register and shifts data onto the SCITXD pin, one bit at a time
- A receiver (RX) and its major registers:
 - RXSHF register – Receiver Shift register. Shifts data in from the SCIRXD pin, one bit at a time
 - SCIRXBUF register – Receiver Data Buffer register. Contains data to be read by the CPU. Data from a remote processor is loaded into the RXSHF register and then into the SCIRXBUF and SCIRXEMU registers
- A programmable baud generator
- Data-memory-mapped control and status registers enable the CPU to access the I²C module registers and FIFOs.

The SCI receiver and transmitter operate independently.

6.8.3 Inter-Integrated Circuit

The I²C module has the following features:

- Compliance with the Philips Semiconductors I²C-bus specification (version 2.1):
 - Support for 1-bit to 8-bit format transfers
 - 7-bit and 10-bit addressing modes
 - General call
 - START byte mode
 - Support for multiple master-transmitters and slave-receivers
 - Support for multiple slave-transmitters and master-receivers
 - Combined master transmit/receive and receive/transmit mode
 - Data transfer rate of from 10 kbps up to 400 kbps (I²C Fast-mode rate)
- One 16-word receive FIFO and one 16-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
 - Transmit-data ready
 - Receive-data ready
 - Register-access ready
 - No-acknowledgment received
 - Arbitration lost
 - Stop condition detected
 - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

Figure 6-21 shows how the I²C peripheral module interfaces within the device.

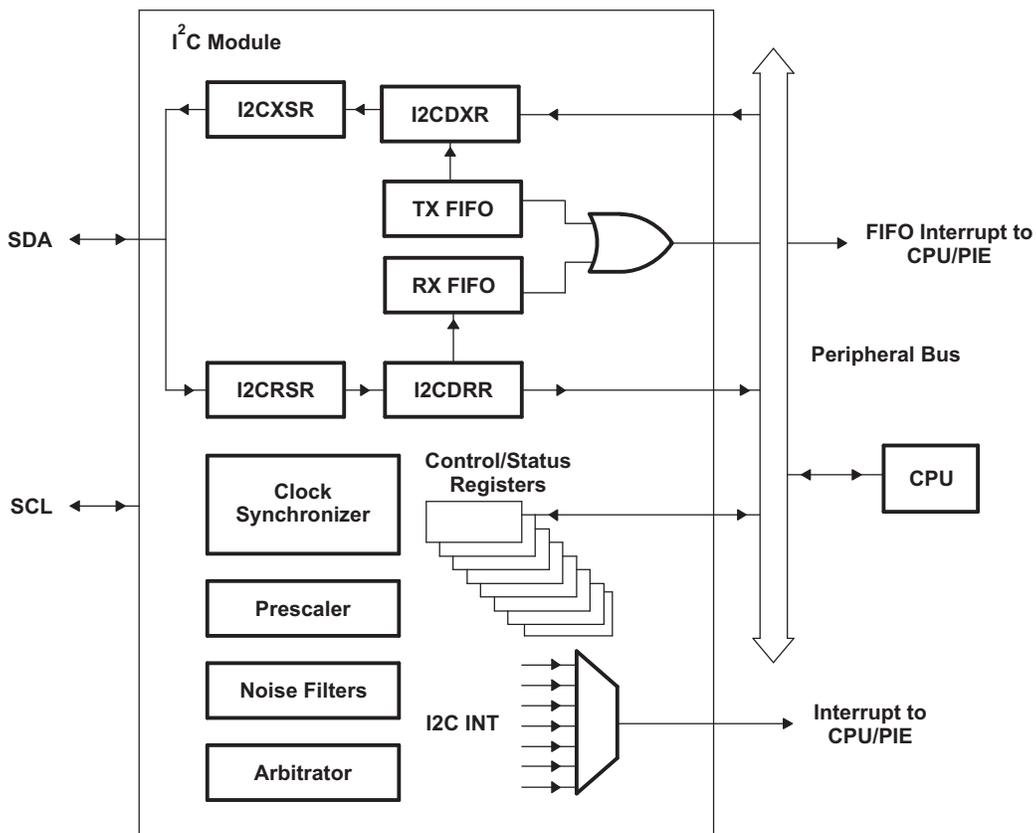


Figure 6-21. I²C Peripheral Module Interfaces

6.8.4 Multichannel Buffered Serial Port

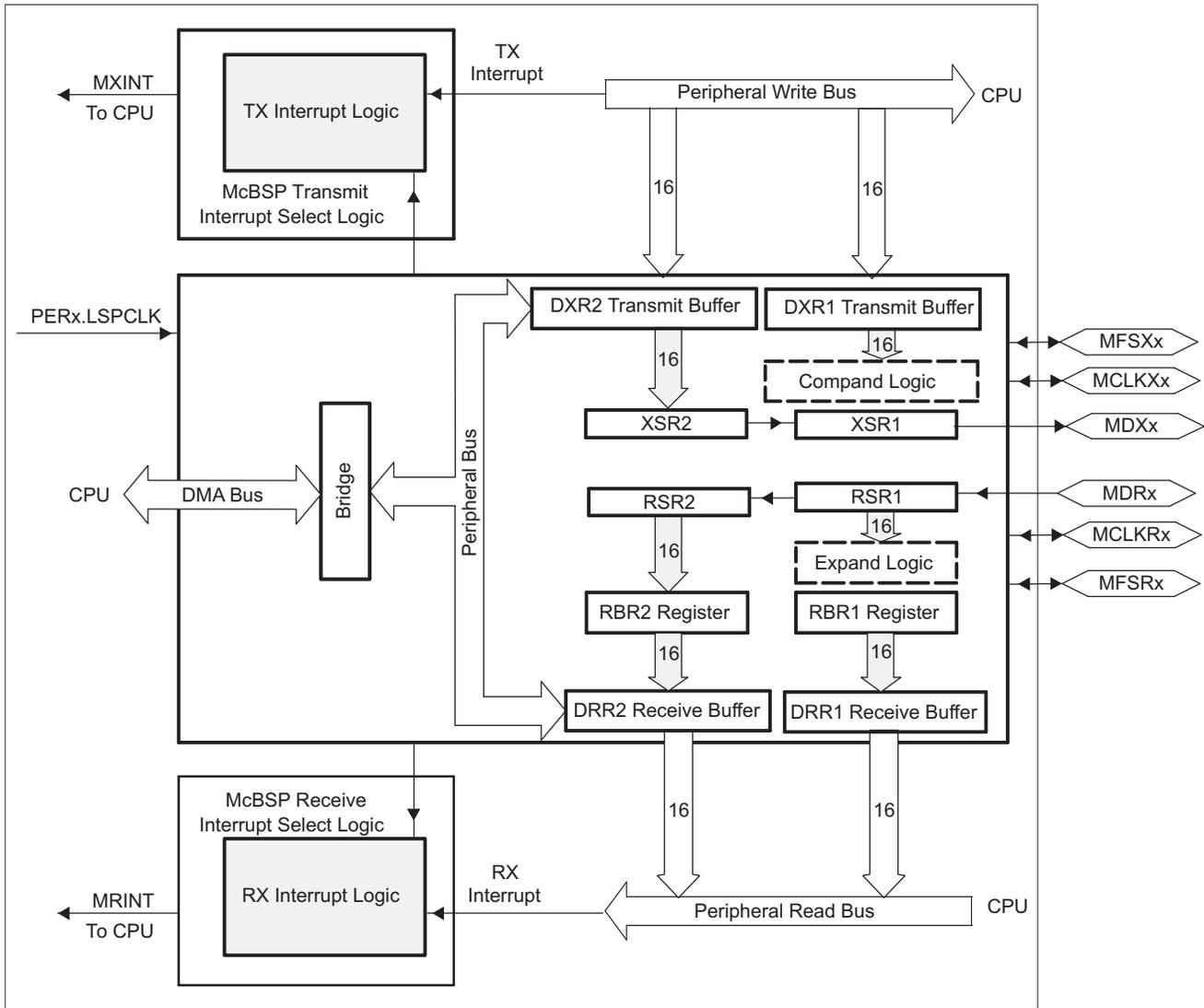
The McBSP module has the following features:

- Compatible to McBSP in TMS320C28x/TMS320F28x DSP devices
- Full-duplex communication
- Double-buffered data registers that allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- 8-bit data transfer mode can be configured to transmit with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected A/D and D/A devices
- Works with SPI-compatible devices
- The following application interfaces can be supported on the McBSP:
 - T1/E1 framers
 - IOM-2 compliant devices
 - AC97-compliant devices (the necessary multiphase frame synchronization capability is provided.)
 - IIS-compliant devices
 - SPI
- McBSP clock rate,

$$\text{CLKG} = \frac{\text{CLKSRG}}{(1 + \text{CLKGDV})}$$

where CLKSRG source could be LSPCLK, CLKX, or CLKR. Serial port performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit.

Figure 6-22 shows the block diagram of the McBSP module.



ADVANCE INFORMATION

Figure 6-22. McBSP Block Diagram

6.8.5 Universal Serial Bus Controller

The USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB host or device functions.

The USB module has the following features:

- USB 2.0 full-speed (12 Mbps) and low-speed (1.5 Mbps) operation
- Integrated PHY
- Four transfer types: control, interrupt, bulk, and isochronous
- 32 endpoints
 - One dedicated control IN endpoint and one dedicated control OUT endpoint
 - 15 configurable IN endpoints and 15 configurable OUT endpoints
- Four KB dedicated endpoint memory: one endpoint may be defined for double-buffered 1023-byte isochronous packet size
- Efficient transfers using DMA controller
 - Separate channels for transmit and receive for up to three IN endpoints and three OUT endpoints
 - Channel requests asserted when FIFO contains required amount of data

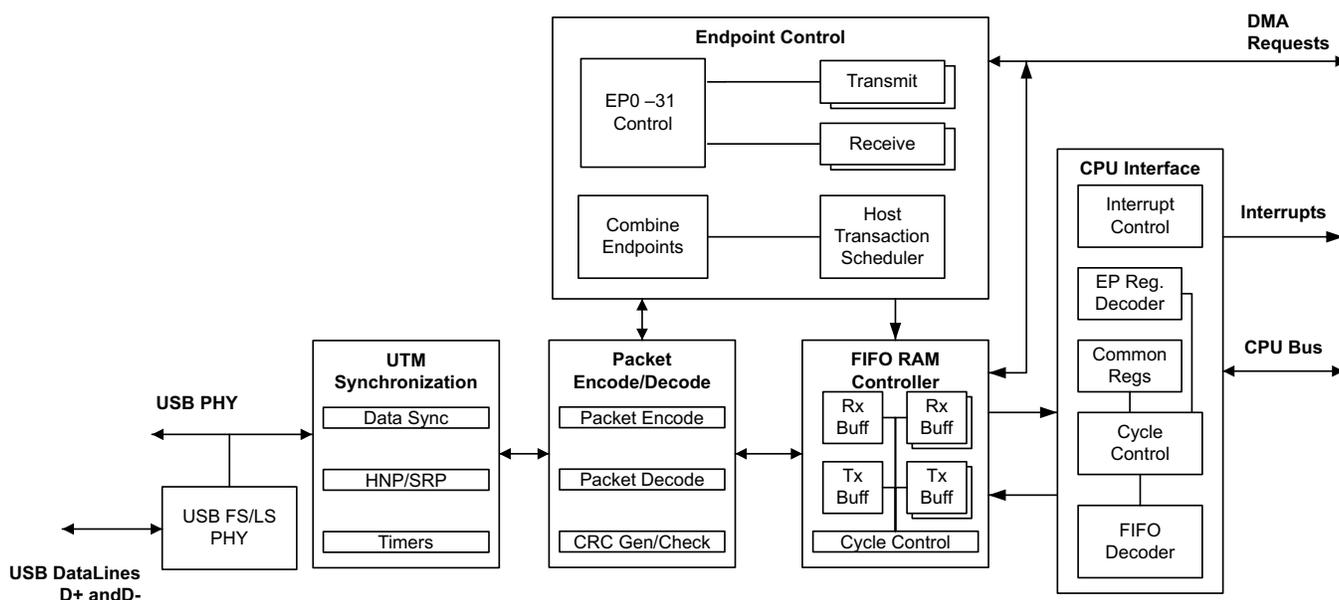


Figure 6-23. USB Block Diagram

6.8.6 Controller Area Network

The CAN module has the following features:

- Fully compliant with CAN protocol, version 2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
 - Configurable as receive or transmit
 - Configurable with standard or extended identifier
 - Has a programmable receive mask
 - Individual identifier mask for each message object
 - Supports data and remote frame
 - Composed of 0 to 8 bytes of data
 - Uses a 32-bit time stamp on receive and transmit message
 - Protects against reception of new message
 - Holds the dynamically programmable priority of transmit message
 - Employs a programmable interrupt scheme with two interrupt levels
 - Employs a programmable alarm on transmission or reception time-out
 - Programmable FIFO mode for message objects
 - Message RAM parity check mechanism
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
 - Operates in a loopback mode receiving its own message. A "dummy" acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

NOTE

For a CANx Bit-CLK of 200 MHz, the smallest bit rate possible is 7.8125 kbps.

6.8.7 External Memory Interface

This EMIF memory controller is compliant with the JESD21-C SDR SDRAMs utilizing a 32-bit/16-bit data bus. The purpose of this EMIF is to provide a means for the CPU to connect to a variety of external devices.

6.8.7.1 Asynchronous Memory Support

The EMIF supports asynchronous memories:

- SRAMs
- NOR Flash memories

There is an external wait input that allows slower asynchronous memories to extend the memory access. The EMIF module supports up to three chip selects (EMIF_CS[4:2]). Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turnaround time
- Extended wait option with programmable timeout
- Select strobe option

6.8.7.2 Synchronous DRAM Support

The EMIF module supports 16-bit/32-bit synchronous DRAM (SDRAM), it has a single SDRAM chip select (EMIF_CS[0]). SDRAM configurations supported are:

- One-bank, two-bank, and four-bank SDRAM devices
- Devices with eight, nine, ten, and eleven column addresses
- CAS latency of two or three clock cycles
- 16-bit/32-bit data bus width
- 3.3-V LVCMOS interface

Additionally, the EMIF supports placing the SDRAM in self-refresh and power-down modes. Self-refresh mode allows the SDRAM to be put in a low-power state while still retaining memory contents; since the SDRAM will continue to refresh itself even without clocks from the microcontroller. Power-down mode achieves even lower power, except the microcontroller must periodically wake up and issue refreshes if data retention is required. Note that the EMIF module does not support mobile SDRAM devices.

7 Device and Documentation Support

7.1 Device Support

7.1.1 Development Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x family of MCUs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development:

Software Development Tools

- Code Composer Studio Integrated Development Environment
 - C/C++ Compiler
 - Code generation tools
 - Assembler/Linker
 - Cycle Accurate Simulator
 - FPU and VCU Optimized Libraries
 - TMU native compiler support
- Application algorithms
- Sample applications code

Hardware Development Tools

- Development and evaluation boards
- JTAG-based emulators - XDS510™ class, XDS560™ emulator, XDS100v2, XDS200
- Flash programming tools

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at www.ti.com. For technical questions, visit <http://e2e.ti.com>. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

7.1.2 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320 MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS320F28377S**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) through fully qualified production devices and tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

- | | |
|------------|--|
| TMX | Experimental device that is not necessarily representative of the final device's electrical specifications |
| TMP | Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification |
| TMS | Fully qualified production device |

Support tool development evolutionary flow:

- | | |
|-------------|---|
| TMDX | Development-support product that has not yet completed Texas Instruments internal qualification testing |
| TMDS | Fully qualified development-support product |

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PTP) and temperature range (for example, S). [Figure 7-1](#) provides a legend for reading the complete device name for any family member.

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F28377S, TMS320F28376S, TMS320F28375S, TMS320F28374S Delfino Microcontrollers Silicon Errata* ([SPRZ422](#)).

ADVANCE INFORMATION

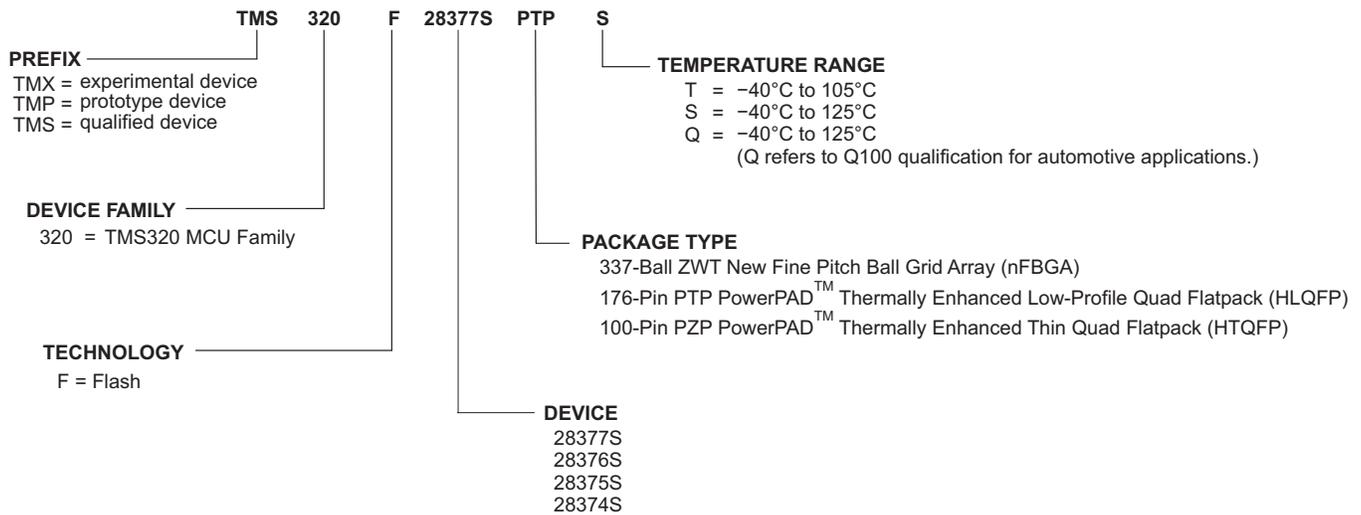


Figure 7-1. Device Nomenclature

7.2 Documentation Support

Extensive documentation supports all of the TMS320 MCU family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications.

The following documents can be downloaded from the TI website (www.ti.com):

Data Manual and Errata

[SPRS881](#) **TMS320F28377S, TMS320F28376S, TMS320F28375S, TMS320F28374S Delfino™ Microcontrollers Data Manual** contains the pinout, signal descriptions, as well as electrical and timing specifications.

[SPRZ422](#) **TMS320F28377S, TMS320F28376S, TMS320F28375S, TMS320F28374S Delfino Microcontrollers Silicon Errata** describes known advisories on silicon and provides workarounds.

Technical Reference Manual

[SPRUHX5](#) **TMS320F2837xS Delfino Microcontrollers Technical Reference Manual** details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the 2837xS microcontrollers.

CPU User's Guides

[SPRU430](#) **TMS320C28x CPU and Instruction Set Reference Guide** describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

[SPRUHS1](#) **TMS320C28x Extended Instruction Sets Reference Guide** describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

[SPRU566](#) **TMS320x28xx, 28xxx DSP Peripheral Reference Guide** describes the peripheral reference guides of the 28x DSPs.

Tools Guides

[SPRU513](#) **TMS320C28x Assembly Language Tools v6.2.4 User's Guide** describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

[SPRU514](#) **TMS320C28x Optimizing C/C++ Compiler v6.2.4 User's Guide** describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

[SPRU608](#) **TMS320C28x Instruction Set Simulator Technical Overview** describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x core.

Application Reports

[SZZA021](#) **Semiconductor Packing Methodology** describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

7.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TMS320F28377S	Click here				
TMS320F28376S	Click here				
TMS320F28375S	Click here				
TMS320F28374S	Click here				

7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Online Community](#) *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#) *Texas Instruments Embedded Processors Wiki*. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.5 Trademarks

Code Composer Studio, PowerPAD, Delfino, TMS320C2000, XDS510, XDS560, TMS320, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

7.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

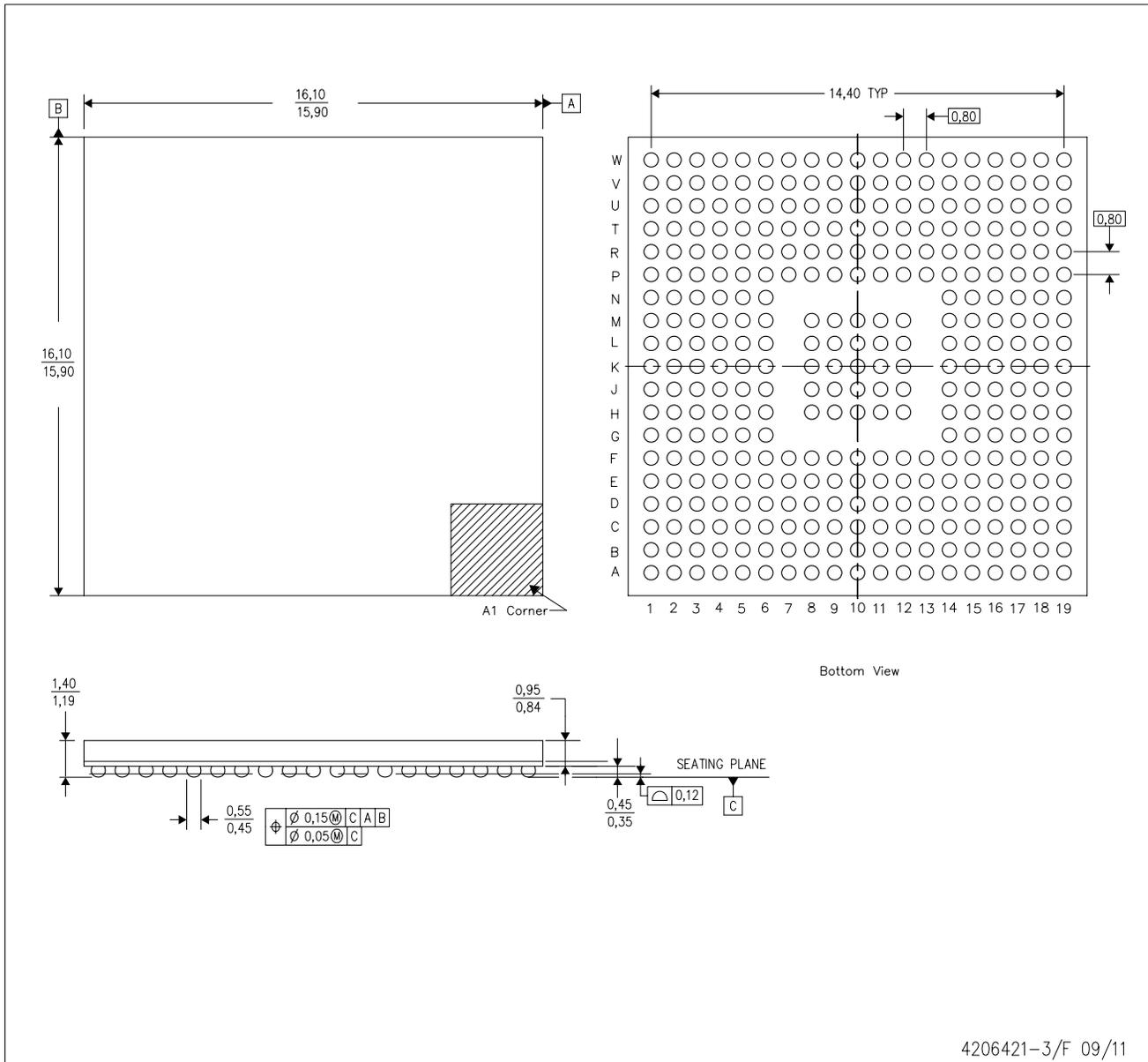
8 Mechanical Packaging and Orderable Information

8.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ZWT (S-PBGA-N337)

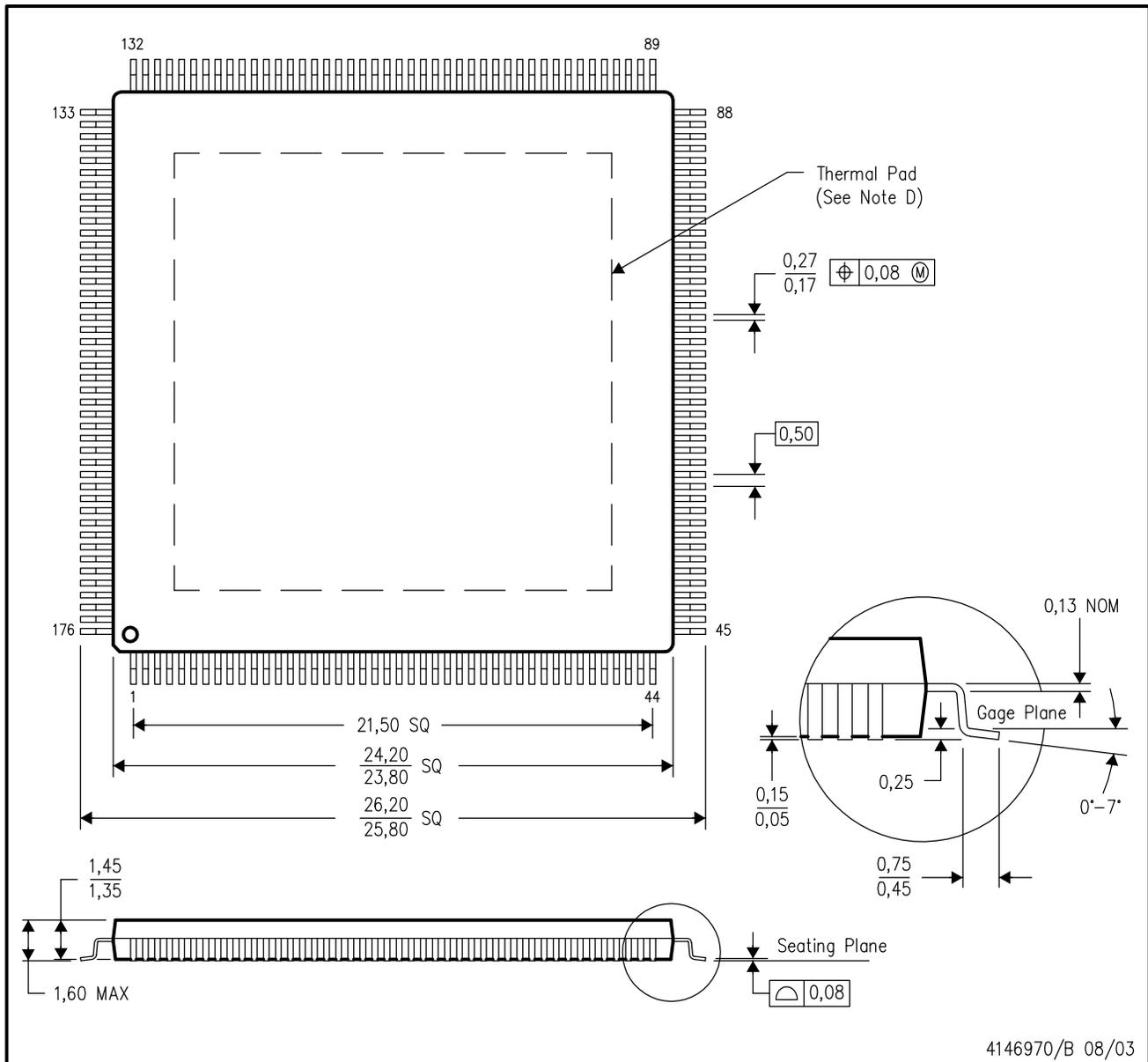
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. This is a Pb-free solder ball design.
 - D. Falls within JEDEC MO-275.

PTP (S-PQFP-G176)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. Falls within JEDEC MO-026

PowerPAD is a trademark of Texas Instruments.

PTP (S-PQFP-G176)

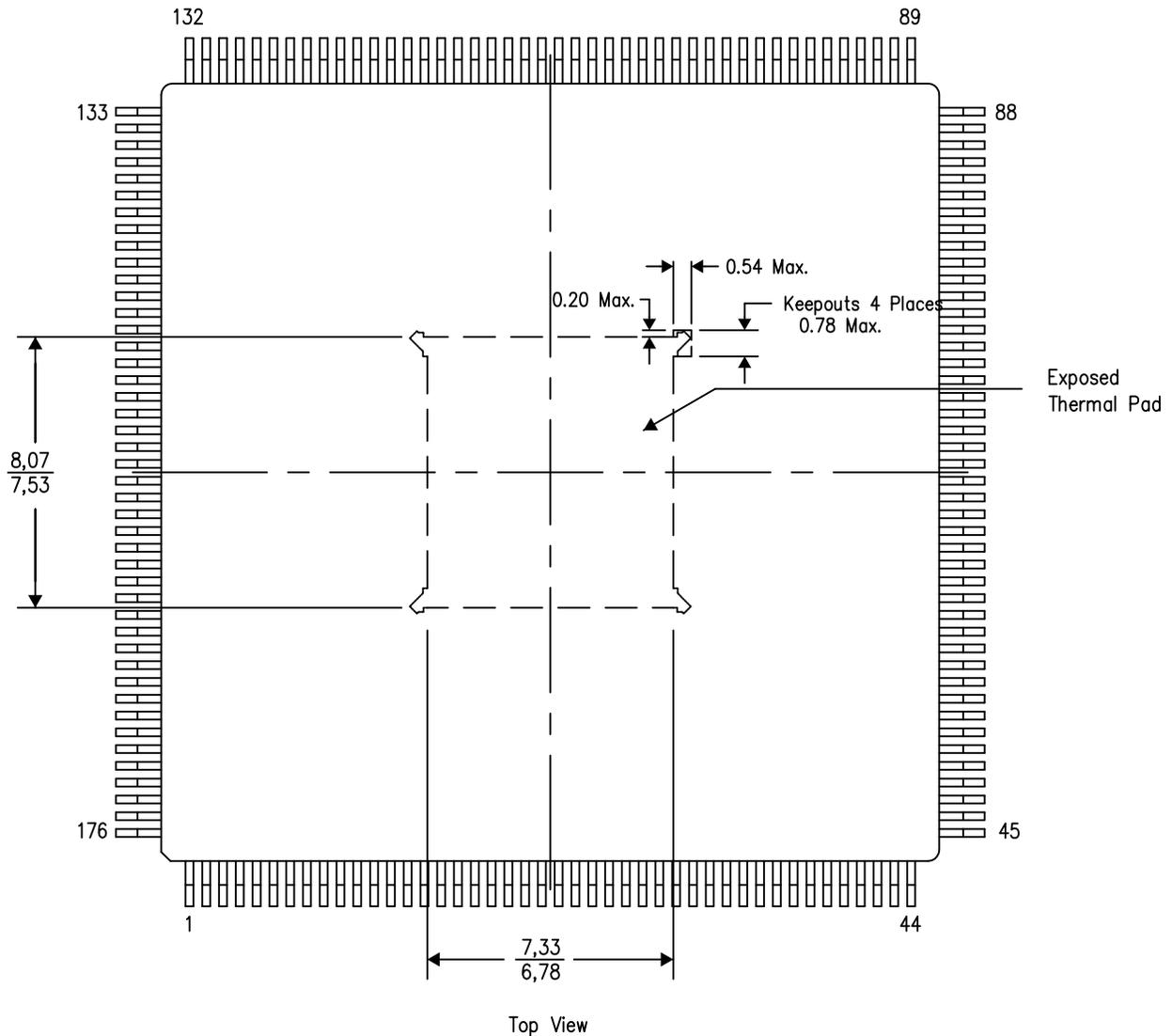
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4209350-8/F 04/13

NOTE: All linear dimensions are in millimeters

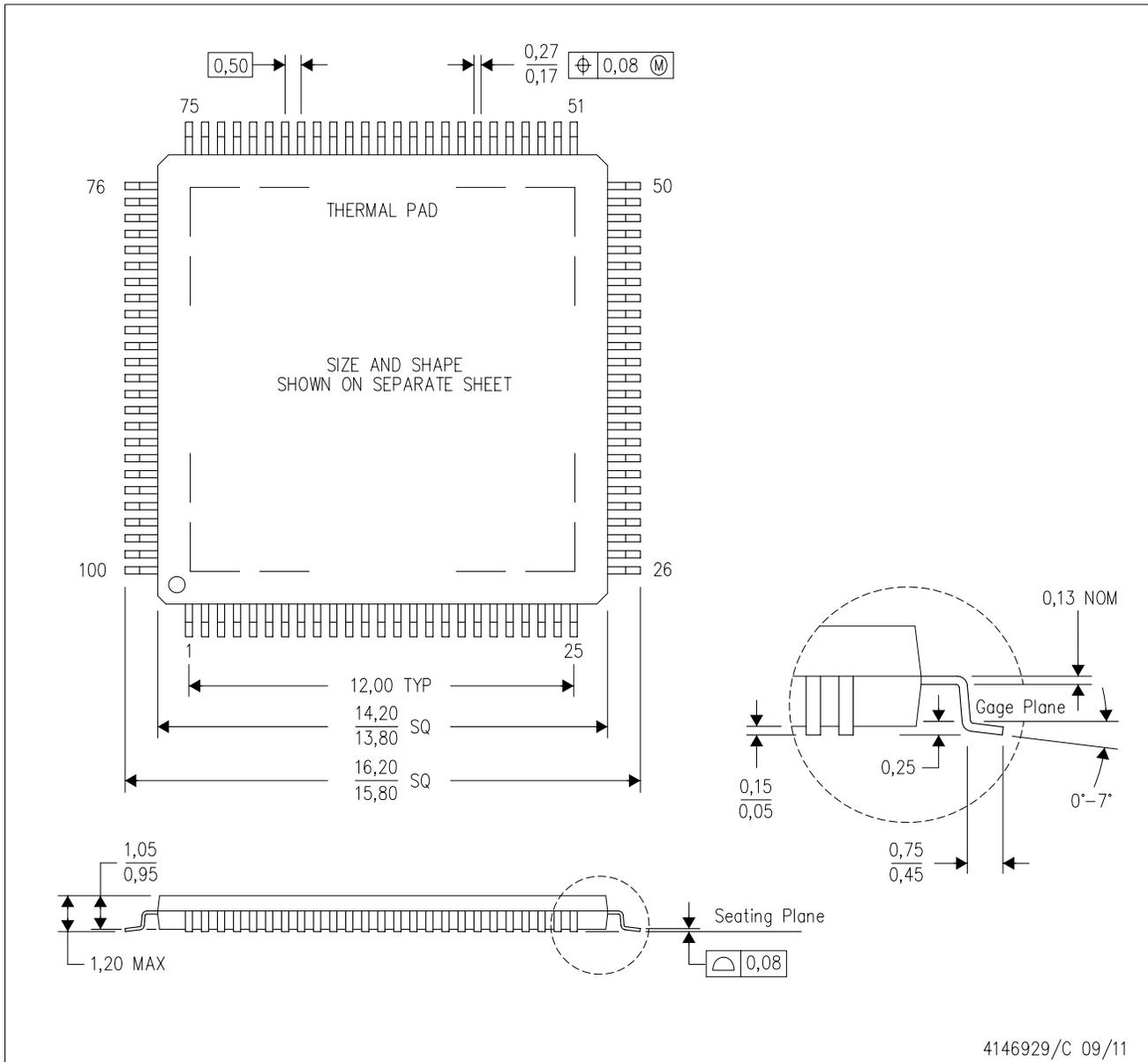
NOTE: Keep-out features are identified to prevent board routing interference. These exposed metal features may vary within the identified area or be completely absent on some devices.

PowerPAD is a trademark of Texas Instruments

MECHANICAL DATA

PZP (S-PQFP-G100)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PZP (S-PQFP-G100)

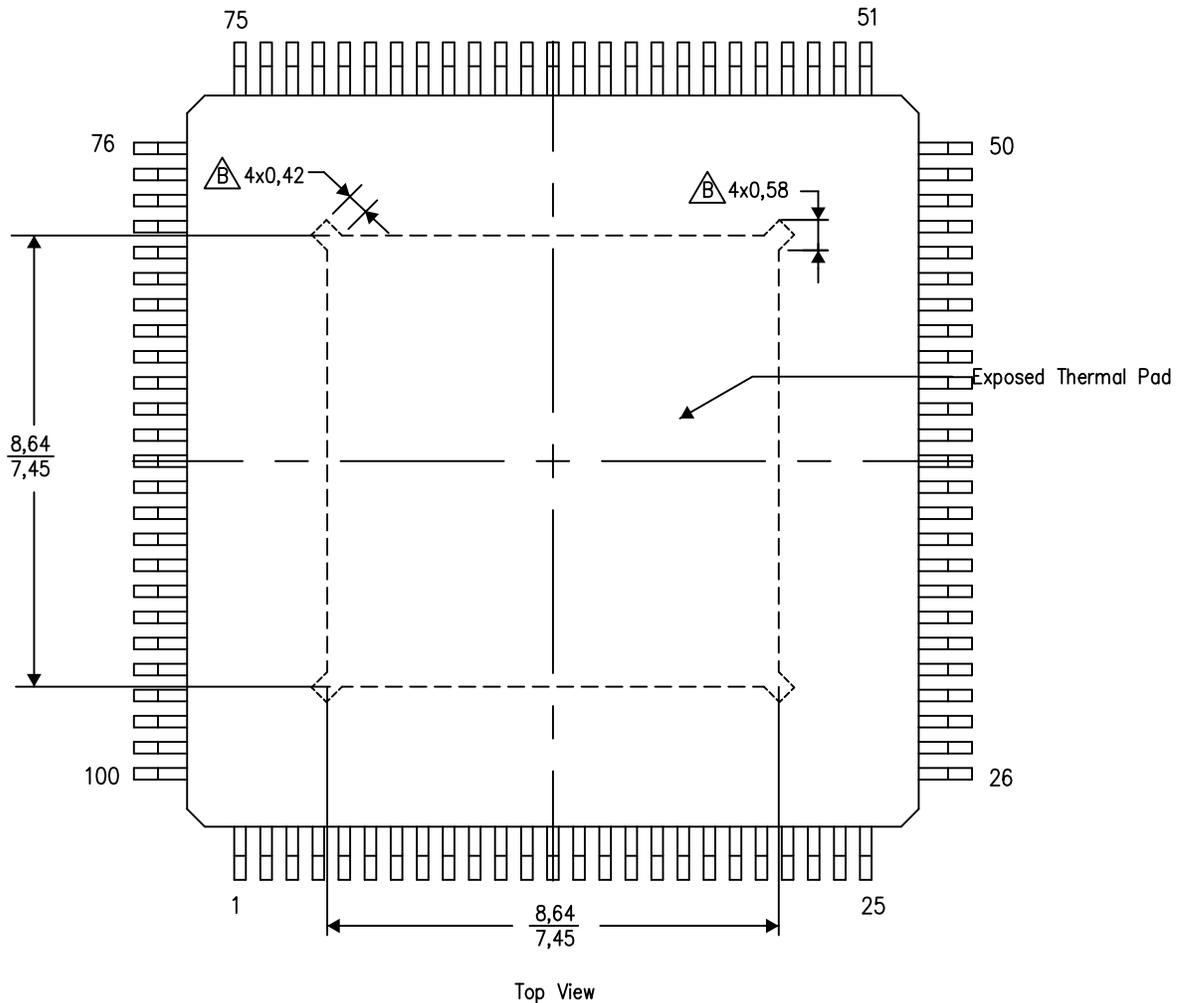
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206333-14/L 05/14

NOTE: A. All linear dimensions are in millimeters

 Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28374SPTPQ	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28374SPTPS	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28374SPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		
TMS320F28374SPZPQ	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28374SPZPS	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28374SPZPT	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28374SZWTQ	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28374SZWTS	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28374SZWTT	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28375SPTPQ	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28375SPTPS	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28375SPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		
TMS320F28375SPZPQ	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28375SPZPS	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28375SPZPT	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28375SZWTQ	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28375SZWTS	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28375SZWTT	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28376SPTPQ	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376SPTPS	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376SPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		
TMS320F28376SPZPQ	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376SPZPS	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376SPZPT	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28376SZWTQ	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376SZWTS	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28376SZWTT	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28377SPTPQ	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377SPTPS	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377SPTPT	PREVIEW	HLQFP	PTP	176	40	TBD	Call TI	Call TI	-40 to 105		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28377SPZPQ	PREVIEW	HTQFP	PZP	100	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377SPZPS	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377SPZPT	PREVIEW	HTQFP	PZP	176	90	TBD	Call TI	Call TI	-40 to 105		
TMS320F28377SZWTQ	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377SZWTS	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 125		
TMS320F28377SZWTT	PREVIEW	NFBGA	ZWT	337	90	TBD	Call TI	Call TI	-40 to 105		
TMX320F28377SPTPT	ACTIVE	HLQFP	PTP	176	1	TBD	Call TI	Call TI	-40 to 105		Samples
TMX320F28377SPZPT	ACTIVE	HTQFP	PZP	100	1	TBD	Call TI	Call TI	-40 to 105		Samples
TMX320F28377SZWTT	PREVIEW	NFBGA	ZWT	337	1	TBD	Call TI	Call TI	-40 to 105		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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